

APPLICATION NOTE

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Written By **Kelley** Engineering DIV

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**F-51852, F-51851, F-51553, F-51405, & F-51320-STEP
Series Graphic Displays**

Approved By Customer



Optrex America, Inc.
46723 Five Mile Road
Plymouth, MI 48170 USA

734.416.8500
www.optrex.com

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REVISION HISTORY

REV	DATE	PAGE	COMMENT
B	4/1/2008	17	Replaced software commands with TABLE 2 to aid comprehension. Added section 5.2.6 & renumbered document from that point forward.
		6	Updated hyperlinks for AVX Elco connectors to Kyocera Elco, Updated Omron part numbers.
		23 - 25	Replaced VLCD and EVR curves to correct voltage and EVR data.
	6/18/2008	9	Updated Table 1 boost ratios to ensure op-amps are not saturated due to low boost voltage. Added 9 and modified 5.2.7 to better explain voltage regulator operation and bypass capacitor selection.
		17	Updated TABLE 2 V5 VOLTAGE REGULATOR RESISTOR RATIO SET command to 0x26 to correct optimal setting. Altered EVR REGISTER SET value to 0x** to highlight the value must be looked up.
		19	Added 6.6.2 to provide guidance for best possible contrast control system and production process design.
	2/25/2009	9	Re-wrote 5.2.6 to establish recommended resistor settings and current dissipation.
		29	Added section 8.0 discussing prototyping parts. Re-numbered remaining sections
		All	Replaced Optrex logo with current version.

1.0 REFERENCES

- (a) [Seiko Epson Document MF424-21 S1D15605 Series Technical Manual](http://w3.epson.com.tw/electronics/PrdSpec/f_2320312311226304479081.pdf)
http://w3.epson.com.tw/electronics/PrdSpec/f_2320312311226304479081.pdf
- (b) [New Japan Radio NJU6676 Specification Ver 2004-03-01](http://www.optrex.com/SiteImages/LitCentral/NJU6676%20Eng.pdf)
<http://www.optrex.com/SiteImages/LitCentral/NJU6676%20Eng.pdf>

2.0 DESCRIPTION

- 2.1. This application note provides guidance for interfacing, programming, and using the F-51320-series, F-51405-series, F-51553-series, F-51851-series, and F-51852-series displays. This document, along with the LCD module specification, the module drawing and LCD controller-driver technical manual, references (a) and (b), provides the application information needed design the display into electronic products. This document IS NOT INTENDED to be the sole source of guidance for using the display.
- 2.2. The LCD module drawing provides size and information for the connector(s) built in the product. The drawing does not provide the mating connector for flexible printed circuits (FPC) since there are many potential sources available.
- 2.3. The LCD Module Technical Specification provides electrical and optical performance specifications, cosmetic specifications, and qualification information. The controller-drivers used in the display can be interfaced in many different configurations and logic voltages. It is not possible to build and test every combination; therefore the specification lists a configuration that was verified by Optrex. This document provides guidance for using various voltage supplies.
- 2.4. The F-51320-, F-51553-, and F-51852-series displays include the following components:

Monochrome liquid crystal display panel. The displays have various color options, which vary by displaying the data image or the inverse data image. Please see FIGURE 1 for examples of each.

 - NJU6676 LCD Controller / Driver (S1D15605 for F-51320, F-51405 & F-51553). References (a) and (b) describe how to use the controller-driver. Optrex highly recommends downloading and studying these before designing hardware and software.
 - RAM to store the digital representation of the image.
 - DC-to-DC Boost Circuit to generate contrast voltage (feature not available on F-51405 & F-51851 displays).
 - Liquid crystal drive circuitry with bias voltage generator and contrast control (via software). This feature not recommended for F-51405 and F-51851 displays.
 - Backlight / Carrier.
- 2.5. The F-51320 operates similarly to the F-51553 and F-51852 but the displays are not exact drop-in replacements for each other. The F-51320 pinout differs from the F-51553 and F-51852 since it does not incorporate the SPI interface. The thickness of some versions of the F-51852 thickness differs from F-51553 and F-51320. For those planning to use one design with various displays, the LCD drive voltages vary between display color modes which may affect software and hardware slightly.
- 2.6. The F-51405 and F-51851 displays increase resolution by using two controller-drivers configured for MASTER - SLAVE operation with each driving one-half of the LCD screen.

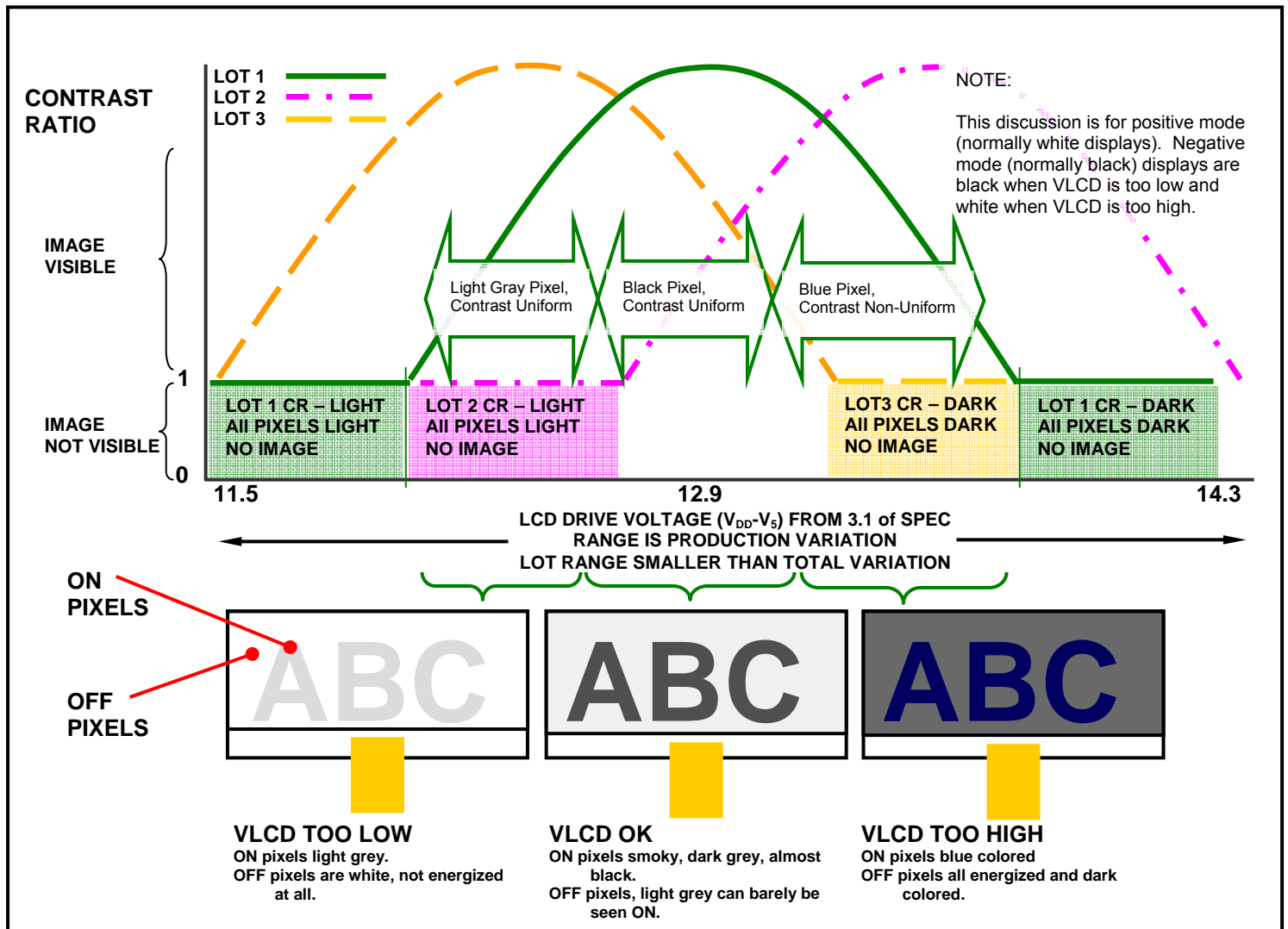
FIGURE 1 -- DISPLAY COLOR AND DATA MODES

F-51851GNFQJ-LB-xxx F-51852GNFQJ-LB-xxx NEGATIVE MODE LCD NORMAL DATA	F-51851GNFQJ-LB-xxx F-51852GNFQJ-LB-xxx NEGATIVE MODE LCD INVERSE DATA
F-51851GNFQJ-LG-xxx F-51852GNFQJ-LG-xxx NEGATIVE MODE LCD NORMAL DATA	F-51851GNFQJ-LG-xxx F-51852GNFQJ-LG-xxx NEGATIVE MODE LCD INVERSE DATA
F-51852GNFQJ-LR-xxx NEGATIVE MODE LCD NORMAL DATA	F-51852GNFQJ-LR-xxx NEGATIVE MODE LCD INVERSE DATA
F-51851GNFQJ-LW-xxx F-51852GNFQJ-LW-xxx NEGATIVE MODE LCD NORMAL DATA	F-51851GNFQJ-LW-xxx F-51852GNFQJ-LW-xxx NEGATIVE MODE LCD INVERSE DATA
F-51852GNFQJ-LY-xx F-51852GNFQJ-LY-xxx NEGATIVE MODE LCD NORMAL DATA	F-51851GNFQJ-LY-xxx F-51852GNFQJ-LY-xxx NEGATIVE MODE LCD INVERSE DATA
F-51852GNBJ-LW-xxx F-51553GNBJ-LW-xxx F-51320GNB-LW-xxx F-51405GNB-LW-xxx NEGATIVE MODE LCD NORMAL DATA	F-51852GNBJ-LW-xxx F-51553GNBJ-LW-xxx F-51320GNB-LW-xxx F-51405GNB-LW-xxx NEGATIVE MODE LCD INVERSE DATA
F-51851GNFJ-SLW-xxx F-51852GNFJ-SLW-xxx POSITIVE MODE LCD NORMAL DATA	F-51851GNFJ-SLW-xxx F-51852GNFJ-SLW-xxx POSITIVE MODE LCD INVERSE DATA

3.0 THEORY OF OPERATION

- 3.1. A microprocessor writes to the LCD controller to configure it for operation send image data. The controller reads the RAM automatically generates voltage waveforms to cause the liquid crystal pixels to change state. There is one data bit in RAM for each pixel location. The controllers in F-51851 & F-51405 must be configured independently to show their portion of the image.
- 3.2. The liquid crystals require a complex, time-changing, high voltage waveform whose magnitude is larger than V_{DD} . This LCD drive voltage may be either internally or externally generated dependent upon the boost capability of the IC and the supplied logic voltage.
- 3.3. The LCD drive voltage is resistance divided to form six discrete voltages applied to the electrical traces on the glass. The difference between the voltage levels corresponds to the display bias ratio. The ON pixel voltages are V_{DD} and V_5 . The OFF pixel voltages are V_1 through V_4 .
- 3.4. Display contrast, the difference in luminance from the ON pixel state to the OFF pixel state, is controlled by varying the magnitude of the LCD drive voltage. Changing the contrast voltage causes all voltages V_1 to V_5 to change. Excessive drive causes the normally OFF voltages to exceed the liquid crystal ON voltage and change state; contrast is reduced. Excessive drive voltage also causes crosstalk as voltage bleeds from ON pixels to OFF pixels. Insufficient voltage prevents the liquid crystals from changing state; no image is seen. FIGURE 2 shows the voltage to contrast ratio relationship and lot to lot variation. The designer must account for this variation.

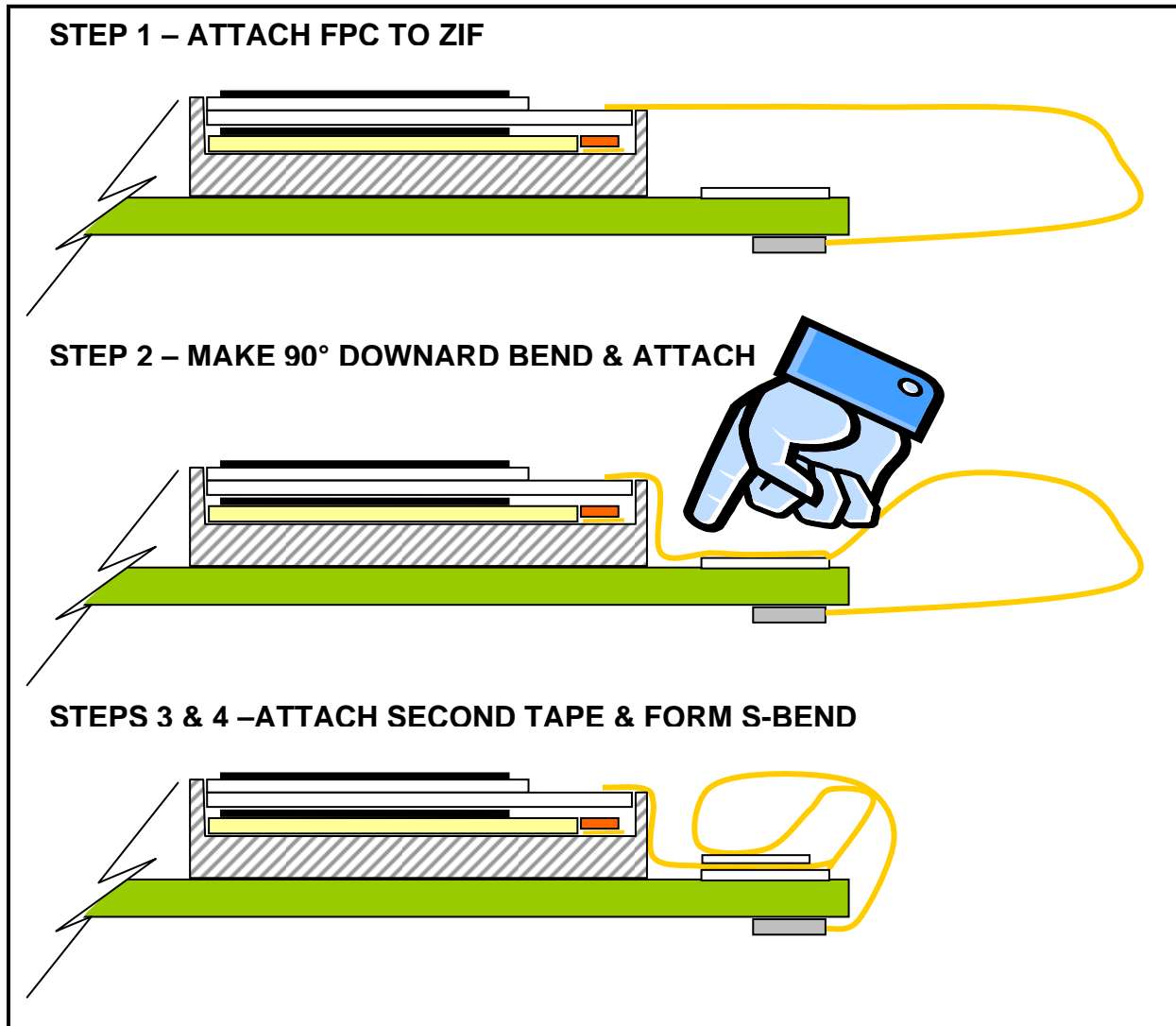
FIGURE 2 -- DISPLAY CONTRAST



4.0 MECHANICAL CONSIDERATIONS

- 4.1. The display may be attached via screws or double sided adhesive. The frame is made of polycarbonate.
- 4.2. The flexible printed circuit (FPC) must not tightly bend and permanently deform the copper traces (form a crease). During bending, the inner side of the copper traces are compressed while the outer side is placed in tension; fracturing the trace and electrically opening the circuit. The minimum bend radius should be 10 times the thickness of the FPC to prevent permanent deformation. The drawing dimensions the FPC as 0.3 mm thick at the stiffener. This is not the thickness where bending occurs. The FPC is 0.120 mm thick in the bend area. The minimum bend radius is 1.2 mm for a 90 degree bend. A 180° bend requires a larger radius to prevent creasing. Small radius bends greater than 90° should be formed ONCE and not unbent.
- 4.3. FIGURE 3 describes a method to bend the FPC and shorten its length. The plastic frame extends 1.2 mm beyond the edge of the glass, so the FPC minimum bend radius allows a bend touching the frame.

FIGURE 3 -- FPC BENDS TO SHORTEN LENGTH.



5.0 ELECTRICAL

5.1. INTERFACE CONNECTION & VOLTAGES

- 5.1.1. The F-51320, F-51553 and F-51852 displays interface via a 30-conductor FPC. A major design consideration is the contact location in the connector. The contacts may be top or bottom. The FPC contacts are on the bottom side. The designer must take FPC bending and connector location into account and choose the correct contact location when selecting connectors. Sources for compatible connectors are:

[Kyocera Elco 08-6210-030-340-800](#) – 30 pin, zero insertion force (ZIF), right angle, bottom contact, surface mount, 0.5 mm pitch FPC, 0.30 mm thick, with front slide lock.

[Molex 54132-3097](#) – 30 pin, zero insertion force (ZIF), right angle, bottom contact, surface mount, 0.5 mm pitch FPC, 0.30 mm thick, with front slide lock.

[Omron XF2M-3015-1A](#) – 30 pin, zero insertion force (ZIF), right angle, top & bottom contact, surface mount, 0.5 mm pitch FPC, 0.30 mm thick, with rear rotary lock.

The F-51405 and F-51851 interface via two 36-conductor FPCs. The FPC contacts are on the bottom side. Sources of compatible connectors are:

[Kyocera Elco 08-6210-036-340-800](#) – 36 pin, zero insertion force (ZIF), right angle, bottom contact, surface mount, 0.5 mm pitch FPC, 0.30 mm thick, with front slide lock.

[Molex 54132-3662](#) – 36 pin, zero insertion force (ZIF), right angle, bottom contact, surface mount, 0.5 mm pitch FPC, 0.30 mm thick, with front slide lock.

[Omron XF2M-3615-1A](#) – 36 pin, zero insertion force (ZIF), right angle, top & bottom contact, surface mount, 0.5 mm pitch FPC, 0.30 mm thick, with rear rotary lock.

These part numbers are presented for information only. Optrex has not tested the performance and reliability of these connectors and makes no warranty to their fitness for use. Please note that any connector matching the FPC pitch characteristics and mating tolerances may be used.

- 5.1.2. The F-51851, F-51852, F-51405 and F-51553 controller/drivers may be configured for 8-bit parallel or 8-bit serial (SPI) communication. This feature is not available on F-51320. Selection of parallel / serial data is controlled by the P/S signal (pin 29 for F-51851 & F-51553, and pin 34 for F-51405 & F-51851). Pull the pin high or low; do not float. Pull the pin HIGH for parallel data input or LOW for serial data. Floating the pin is known to cause timing issues.. See reference (a) page 8-25 and reference (b) page 30.

Pins 11 to 16 (D0 to D5) – no connect

Pin 17 D6 – Serial clock (SCL)

Pin 18 D7 – Serial data (SI)

Using SPI prevents reading the display status and RAM. It is advantageous to use the parallel interface during development in order to read the controller status and RAM. Switch to SPI after confirming EMI / EMC and ESD compatibility.

- 5.1.3. The F-51320, F-51553, & F-51852 require resistors attached to the VR pin to set the voltage regulator gain as shown in FIGURE 5. The F-51553 and F-51320 use the S1D15605 controller driver and have the option of using internal resistors. To select this option, pull pin 30 HIGH. If not using the internal resistors pull LOW. The F-51852 requires external resistors and pin 30 is not connected.

- 5.1.4. The following connections apply to the F-51405 and F-51851.

Pins (2) FR, (3) CL, (4) DOF – The MASTER outputs clock and frame signals to the SLAVE for synchronization purposes. These pins should be connected together from the MASTER to SLAVE using the shortest possible path length to minimize capacitance that can distort

the timing waveforms. The DOF pin allows the MASTER to control the SLAVE output driver pins ON and OFF.

Do not connect the boosting capacitor pins (22 to 26).

Pin (35) IRS [F-51405 ONLY] – The IRS pin controls the use of internal resistor values used for the DC-to-DC boost converter. This converter is not used since an external power supply will be used to create the LCD drive voltages. Pin 35 (IRS) should be set low for the MASTER. The IRS pin should not be connected for the SLAVE. The SLAVE pin is pulled to V_{DD} on the glass. Setting the SLAVE IRS low will cause the display contrast to vary by quadrant.

The controller-driver is selected when CS1 is low and CS2 is high. Please note the MASTER and SLAVE must not be selected simultaneously when writing data or commands.

5.2. LOGIC AND LIQUID CRYSTAL POWER SUPPLIES

- 5.2.1. The display specification lists the logic voltage at which Optrex confirmed operation, but the IC may operate at other logic voltages listed in references (a) and (b). When other logic voltages are used, the designer must set V_5 appropriately to generate the $V_{DD}-V_5$ voltage difference to run the liquid crystals. This voltage is specified in Section 3.1 of the LCD specification.
- 5.2.2. The S1D15605 and NJU6676 are negatively biased; V_{DD} is used as the reference voltage. The difference between V_{DD} and the LCD drive voltage ($V_{DD}-V_5$) must meet the requirements of Section 3.1 of the LCD specifications. FIGURE 4 provides an example of the LCD driving voltage requirement.

Contrast voltage may be controlled via several methods depending upon the power supply setup. Power supply setup is discussed in sections 5.2.3 through 5.2.10

Section 3.1 also provides the production variation for VLCD. This means the system design must provide the range of drive voltages in order to obtain proper operation. If the $V_{DD}-V_5$ voltage is fixed, say at 12.9 V, a display that requires 13.3 V to operate will not show an image (see FIGURE 2). By ensuring the system design can provide the maximum voltage at low temperature and the minimum voltage at high temperature, production variation is accommodated. Please design the system to provide variable LCD drive voltage.

Please note the temperature dependence of the liquid crystals. As temperature increases the viscosity of the liquid crystals decreases and less voltage is required to cause the liquid crystal to change state. The drive voltage must be reduced or else contrast will be reduced. As temperatures decrease, the voltage must be increased. The S1D15605 has -0.05 % temperature compensation of V_5 . The NJU6676 does not have automatic temperature compensation so the electronic volume should be varied to control contrast. See Section 6.6 for recommended settings.

FIGURE 4 -- LCD DRIVING VOLTAGE VS TEMP

3. Optical Specifications						
3.1. LCD Driving Voltage						
Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Recommended LCD Driving Voltage Note 1	$V_{DD}-V_5$	Ta= -20°C	-	-	14.3	V
		Ta=25°C	12.0	12.9	13.8	V
		Ta=70°C	11.5	-	-	V

Note 1 : Voltage (Applied actual waveform to LCD Module) for the best contrast. The range of minimum and maximum shows tolerance of the operating voltage. The specified contrast ratio and response time are not guaranteed over the entire range.

5.2.3. FIGURE 5 shows the NJU6676 and S1D15605 LCD drive voltage generating circuits. The ICs features include:

- A DC-to-DC boost circuit for generating a large negative voltage available on V_{OUT} . V_{OUT} is supplied to the voltage regulator op-amp as one rail voltage. V_{DD} is the other rail voltage. If desired, the designer may supply V_{OUT} externally. An external V_{OUT} must meet: $V_{DD} - V_{OUT} > (MAX [V_{DD} - V_5] + 0.1 V)$.
- A voltage regulator. This circuit can adjust the magnitude of the LCD drive voltage, $V_{DD}-V_5$, to control contrast by setting an internal register value via software. The designer also has the option to provide this voltage externally to the V_5 pin.
- A voltage follower. This circuit generates the six drive voltages needed to run the liquid crystals. If desired, the designer may supply the six voltages externally. See Section 5.2.10.

There are eight possible combinations of these features. In practice, there are three practical combinations based upon the V_{DD} , boost capability, and the required liquid crystal drive voltage.

POWER CONTROL OPTION 1 – DC-to-DC Boost ON, Voltage Regulator ON, Voltage Follower ON. Recommended for F-51320 and F-51553 displays.

POWER CONTROL OPTION 2 – DC-to-DC Boost OFF, Voltage Regulator ON, Voltage Follower ON. Recommended for F-51852 displays.

POWER CONTROL OPTION 3 – DC-to-DC Boost OFF, Voltage Regulator OFF, Voltage Follower OFF. Recommended for F-51405 and F-51851 displays.

5.2.4. The F-51320 and F-51553 have sufficient boost capability to use the internal DC-to-DC booster, voltage regulator and voltage follower. This provides software control of contrast and the absolute minimum component count. TABLE 1 provides the possible combinations of V_{DD} and DC-to-DC boost ratio. FIGURE 6 provides the boost capacitor configuration.. FIGURE 7 shows the typical hookup.

FIGURE 9 shows the external power supply option. Use this hookup for least flicker.

TABLE 1 -- F-51320- & F-51553-SERIES DC BOOST BY $V_{DD}-V_{SS}$

PART NUMBER	1.8	2.2	2.5	2.8	3.0	3.3	5.0
F-51553GNBJ-LW-AEN	EXT	EXT	INT 4X	INT 4X	INT 4X	INT 4X	INT 3X
F-51320GNB-LW-AEN	EXT	EXT	INT 4X	INT 4X	INT 4X	INT 4X	INT 3X
F-51320GNF-AC	EXT	EXT	INT 4X	INT 4X	INT 4X	INT 4X	INT 3X
F-51320GNY-LY-AFN	EXT	EXT	INT 4X	INT 4X	INT 4X	INT 4X	INT 3X

CAUTION:

DO NOT USE 4x BOOST WITH A 5 V $V_{DD}-V_{SS}$. THE BOOSTED VOLTAGE EXCEEDS THE ABSOLUTE MAXIMUM RATING FOR THE V_{OUT} PIN OF THE IC.

5.2.5. The F-51852 DC-to-DC boost circuit does not have sufficient boost capability to reliably drive the liquid crystals over the entire VLCD operating range (except for 5 V V_{DD}). For these cases, the DC-to-DC boost circuit should not be used. A negative voltage should be applied to the V_{OUT} pin. By supplying a voltage to V_{OUT} , the voltage regulator and voltage follower can be used for software control of contrast and to minimize component count.

For 5 V V_{DD} , hook up the display as shown in FIGURE 7. If unacceptable flicker occurs, hook up the display as shown in FIGURE 8. For V_{DD} other than 5 V, use FIGURE 8.

FIGURE 9 shows the external power supply option. Use this hookup for least flicker.

FIGURE 10 provides a typical schematic hookup using an external supply to the V_{OUT} pin.

5.2.6. S1D15605 and NJU6676 both control contrast via the ELECTRONIC VOLUME REGISTER (EVR) setting in software. The internal voltage regulator gain $[(1 + (R_B / R_A))]$ sets the control range. The graphs at the end of this document provide optimal EVR settings with 3.3 V V_{DD} ; The gain must be calculated from formulas in references (a) and (b) for other V_{DD} .

Choosing $R_A = 330 \text{ K}\Omega$ and $R_B = 1.33 \text{ M}\Omega$ yields a gain of five and allows EVR setting to control contrast over the entire temperature range.

$V_{DD}-V_5$ from Table 3.1 of the display specification is the voltage drop across R_A and R_B . The current is $(V_{DD} - V_5) / (R_A + R_B)$.

5.2.7. Use the following values for the boost and bypass capacitors (see FIGURE 6 through FIGURE 8):

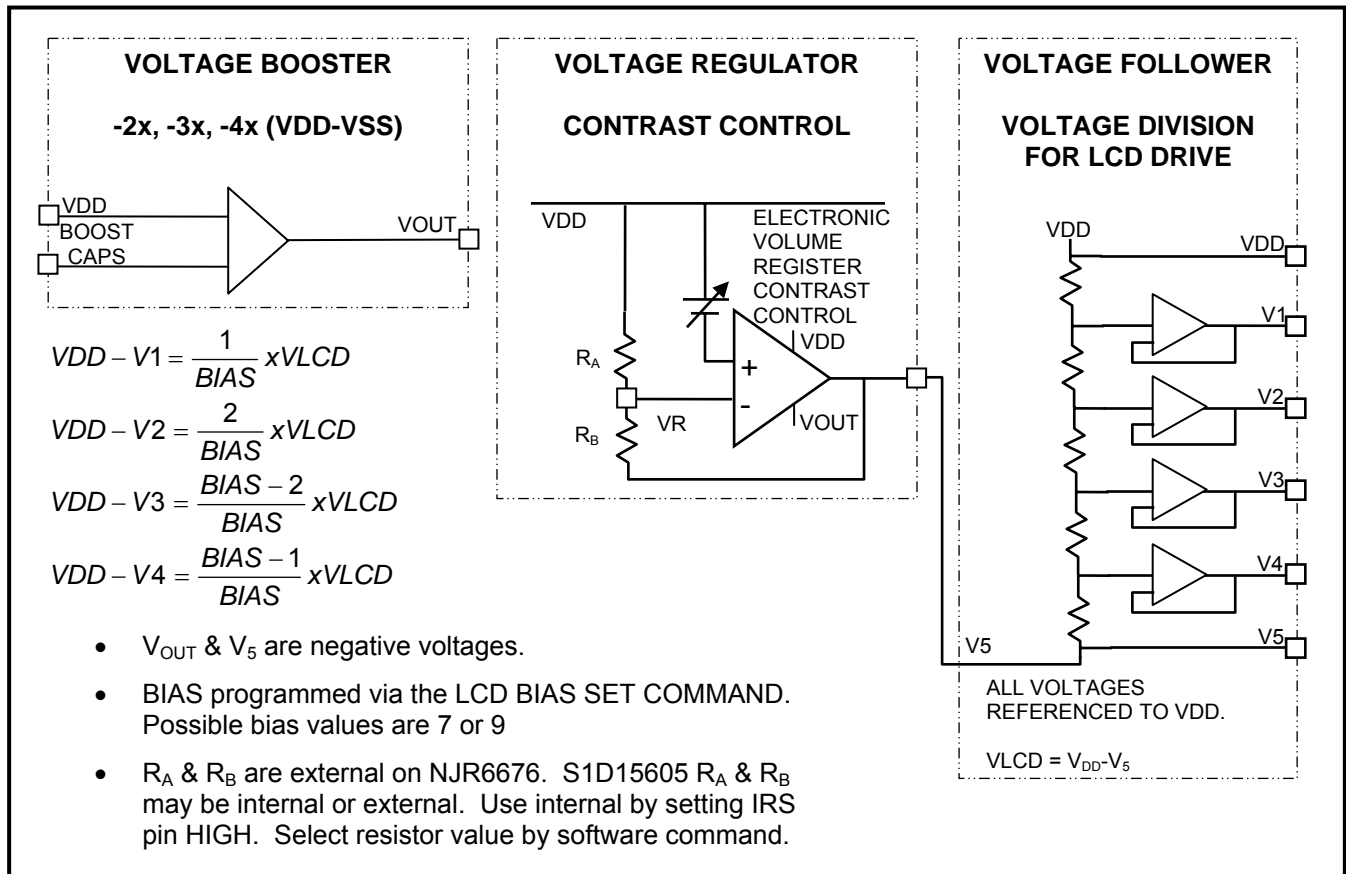
Boost capacitors (C1) – 1.0 μF to 4.7 μF

Bypass capacitors (C2)– 0.1 μF to 1.0 μF

The voltage differences between V_5-V_4 , V_4-V_3 , V_2-V_1 and V_1-V_{DD} should be equal. The magnitude is the bias voltage difference (see equations in FIGURE 5). If the display has uneven pixel contrast, increase the size of the C2 capacitors to stabilize the voltage. Determine the C2 value by displaying a heavy load image (such as horizontal stripes) and selecting a value that stabilizes the liquid crystal driven voltages (V_1 to V_5) and minimizes pixel color difference and flicker. Note that all capacitors must have the same capacitance value.

5.2.8. The F-51405 and F-51851 use two controllers in MASTER – SLAVE setup. The DC-to-DC boost is permanently disabled on the SLAVE. The MASTER does not have sufficient drive to run the display – an external power supply generating V_1 to V_5 supply for both ICs is required. Optrex does not recommend using the internal voltage regulator and follower. IC Production variation cause slight voltage differences and contrast variation by display quadrant. Use the external contrast control to ensure contrast uniformity.

FIGURE 5 -- NJU6676 / S1D15605 LCD DRIVE CIRCUITRY



5.2.9. VOLTAGE BOOST SETUP

FIGURE 6 -- VOLTAGE BOOST CONFIGURATION

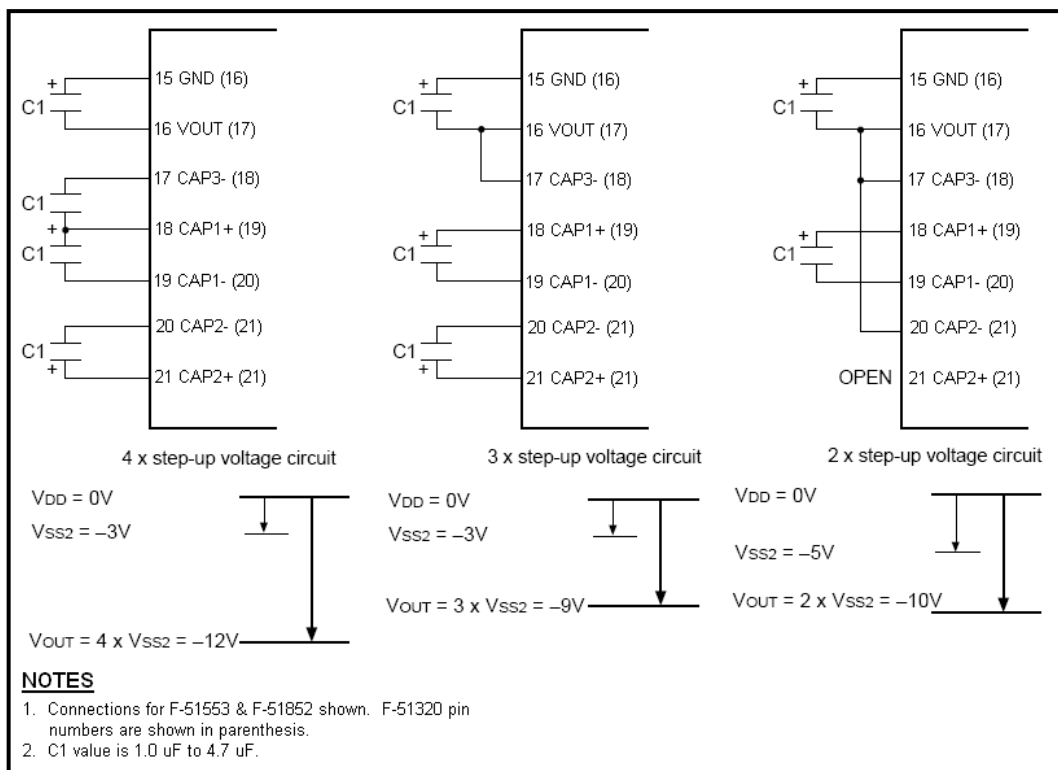


FIGURE 7 – SETUP FOR INTERNAL DC BOOST, VOLTAGE REGULATOR & FOLLOWER

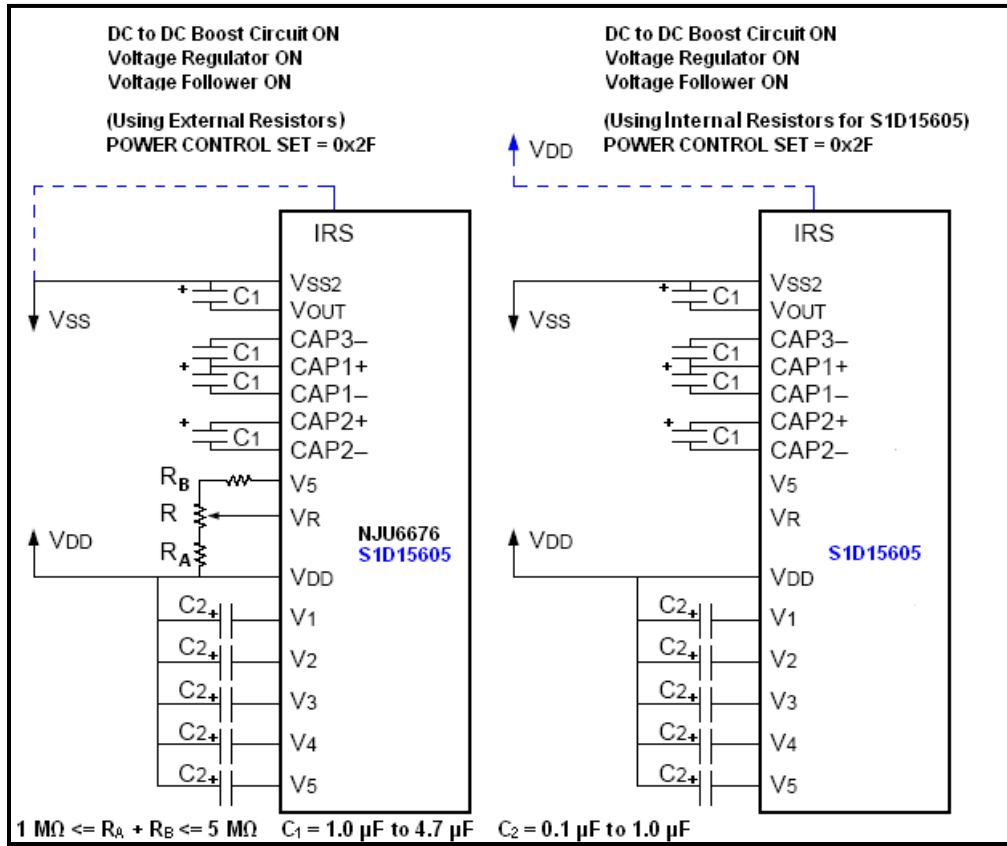
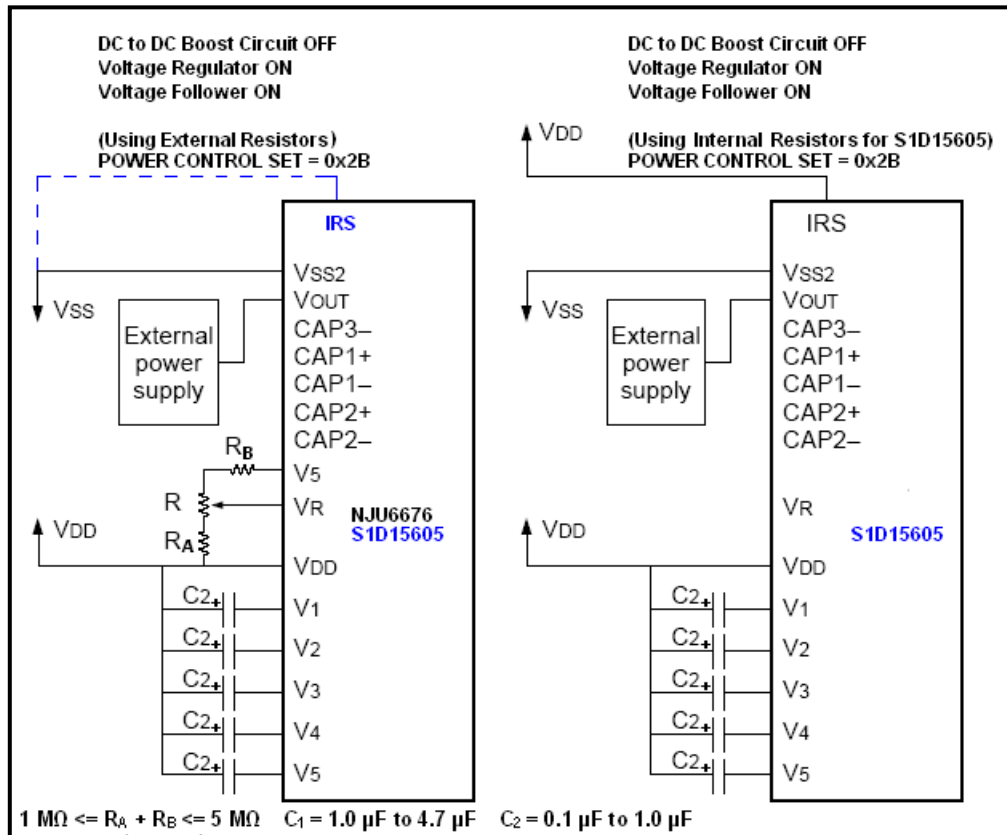


FIGURE 8 – SETUP FOR EXTERNAL DC BOOST, VOLTAGE REGULATOR & FOLLOWER



5.2.10. FIGURE 9 provides a reference power supply design for an external power supply. In this configuration, the electronic volume control is physically bypassed and contrast control via software command is prevented. Display contrast is controlled by varying the magnitude of V_5 . R1 through R5 generate the bias voltages. This power supply is required for the F-51405 and F-51851 displays. Keep the traces between the outputs and the displays short. Long traces add resistance which creates voltage differences between the MASTER and SLAVE drive circuits which causes non-uniform contrast.

FIGURE 9 -- F-51320, F-51405, F-51553, F-51851 & F-51852, EXTERNAL POWER SUPPLY

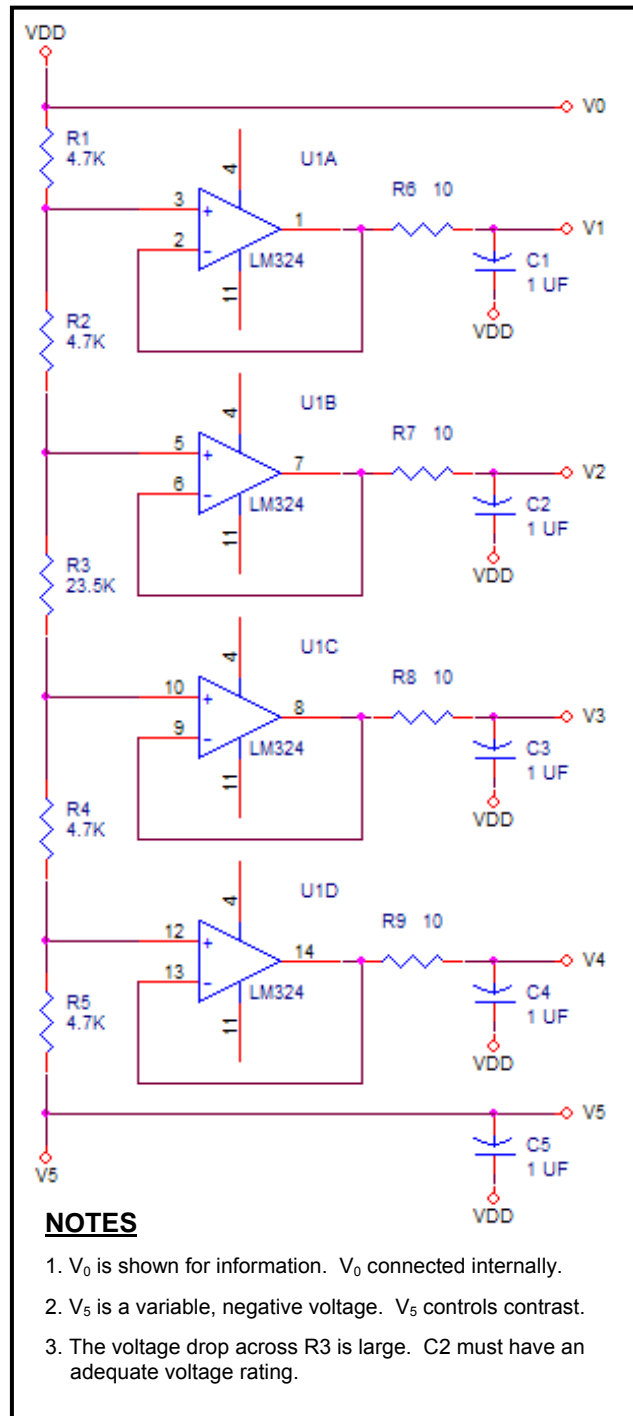
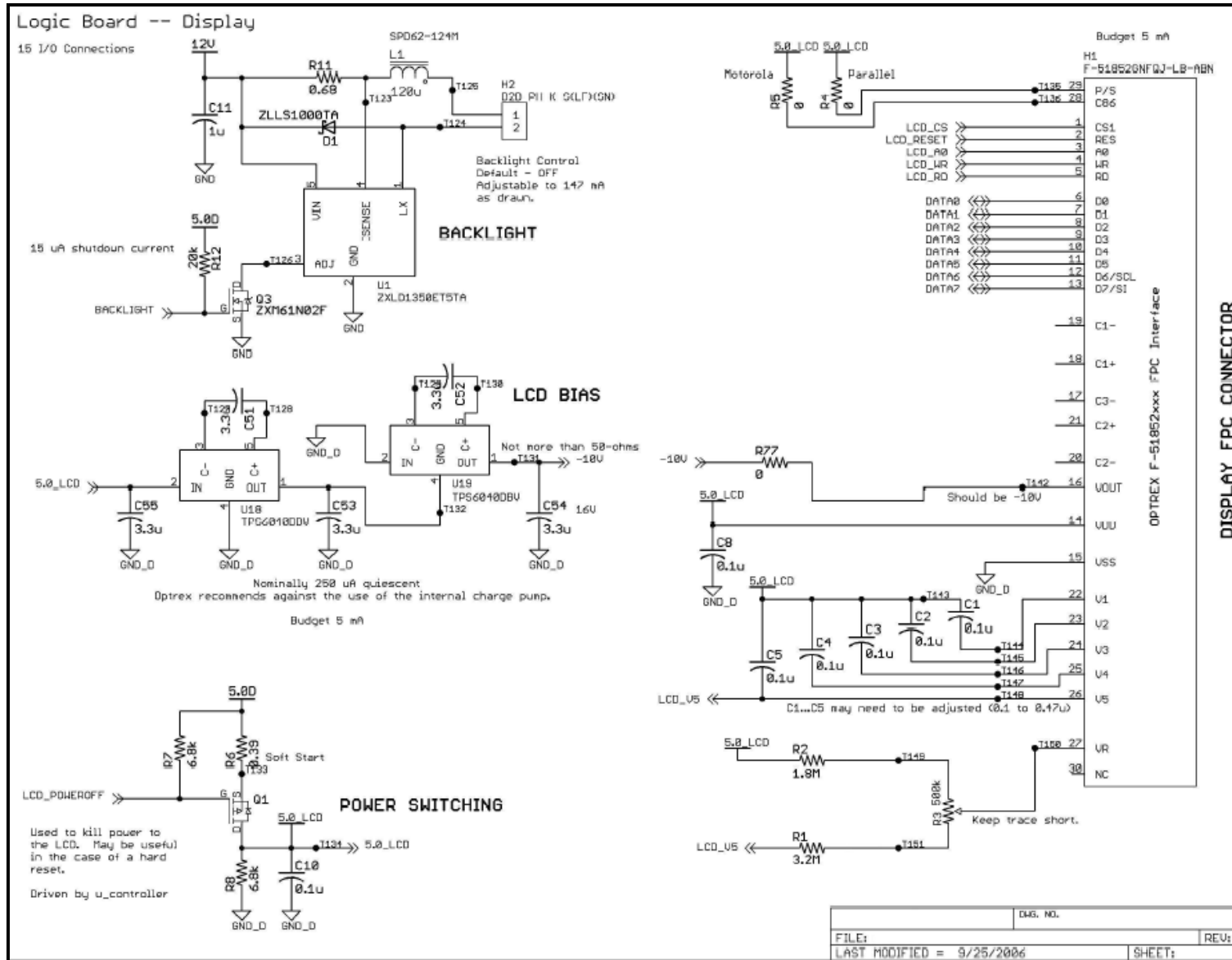


FIGURE 10 -- EXTERNAL SUPPLY TO VOUT & USE INTERNAL VOLTAGE REGULATOR & FOLLOWER



5.3. SIGNAL TIMING

- 5.3.1. S1D15605 timing varies with the operating voltage. Please consult references (a) and (b) if you intend to use V_{DD} other than that listed in the LCD module specification.
- 5.3.2. RESET duration is important; please follow the LCD module specification guidance. If RESET is not held low for the correct time, abnormal operation is possible.
- 5.3.3. The controller-driver instructions require some time to execute. While instructions are executing, commands and data should not be sent. The status of the controller can be read with a parallel interface by using the STATUS READ command to return the BUSY FLAG value. If the software design does not examine this bit, the T_{CYC} requirements must be met to ensure adequate time for the controller to act upon commands. See pages 8-25 and 8-26 of reference (a) and page 31 of reference (b).

5.4. BACKLIGHT

- 5.4.1. The F-51405, F-51851 and F-51852-series backlights use a JST PHR-2 connector. This is a removable, 2 mm pitch, crimp pin connector using the PHR-2 housing. The mating connector is a 2-pin header.

[JST S 2B-PH-SM3-TB](#) – 2-pin, surface mount, side entry, shrouded header, 2 mm pitch.

The mechanical drawing schematic shows resistors; these are populated with zero ohm values. The designer must limit drive current.

- 5.4.2. The transmissive and transfective versions of the F-51320- and F-51553-series have solder pads for connecting backlight drive circuitry. Limit the soldering temperature to 260° C for three seconds. The mechanical drawing schematic shows resistors; these are populated with zero ohm values. The designer must limit drive current.
- 5.4.3. If the designer must limit drive current to protect the LEDs, the current-limiting resistor must meet the criteria of EQUATION 1 and have adequate power rating.

EQUATION 1 – CURRENT LIMITING RESISTOR CALCULATION

$$\frac{V_{SUPPLY} - V_f}{R} \leq I_f$$

The values of V_f and I_f are found in Section 2.4. of the LCD Module Technical Specification. PWM techniques may be used to control luminance. The high temperature current deratings must be followed.

5.5. POWER SUPPLY SEQUENCING & SIGNAL TRANSIENTS

- 5.5.1. The external power supply should be sequenced so that the voltage comes up after V_{DD} at startup and shuts down before V_{DD} at power down. This sequencing should be maintained for inadvertent power down as well. The sequencing relationship depends upon the V_1 to V_5 capacitance and V_{DD} . See reference (a) pages 8-58 through 8-63 and Figure 29. For F-51852 see reference (b) pages 12, 22, and 33.
- 5.5.2. When supplying VLCD externally, the RESET pin should be held LOW while powering on the VLCD supply.
- 5.5.3. The backlight drive voltage should be energized after the LCD is configured and placed in operation to hide optical effects caused by startup with undefined data in the RAM. Likewise, the backlight should be powered OFF before the the display during shutdown.

6.0 SOFTWARE

- 6.1. Each data bit of RAM corresponds to pixel location in the display. This means the display can generate monochrome images by setting the value of a data bit to 1 or 0.

The RAM is organized into 8 bit tall “pages” corresponding to the commons (horizontal lines) on the display. An 8-bit data write maps to 8 pixels in a vertical column. A specific RAM location is selected by specifying the PAGE ADDRESS SET to specify the vertical location and the COLUMN ADDRESS SET to specify the horizontal location.

Reference (a) pages 8-27 and 8-28 and reference (b) pages 10 and 11 discuss the LCD controller RAM operation. The mapping of pixels to RAM is shown in FIGURE 11.

- 6.2. The procedure for writing to the display is:

Execute a PAGE ADDRESS SET to specify the 8-bit vertical location of the data write.

Execute a COLUMN ADDRESS SET to specify the horizontal location.

Execute a DATA WRITE command. The RAM pointer increments automatically.

Execute additional data writes until the RAM reaches the end of a line.

Set the PAGE ADDRESS SET and COLUMN ADDRESS SET as needed to continue.

The COLUMN ADDRESS SET must be executed as the pointer does not automatically reset upon reaching the end of the line.

The ADC SET command controls the direction of the RAM write.

Given the pixel mapping of FIGURE 11, a left to right and up to down image scan requires setting the ADC SELECT register value to \$0xA1 to reverse the horizontal scan and the COMMON OUTPUT MODE SELECT register value to \$0xC8 to reverse the vertical scan.

- 6.3. Unused RAM locations in the S1D15605 may be used for scratchpad memory. Unused RAM locations are:

- PAGES 1 to 7 Column Addresses \$0x80 to \$0x83 (ADC = 1) or \$0x00 to \$0x02 (ADC = 0)
- PAGE 8. These are single bits that can be used for controlling icons (not implemented in the display).

FIGURE 11 – F-51320, F-51553 & F-51852 PIXEL TO RAM MAPPING & ITO CONNECTIONS

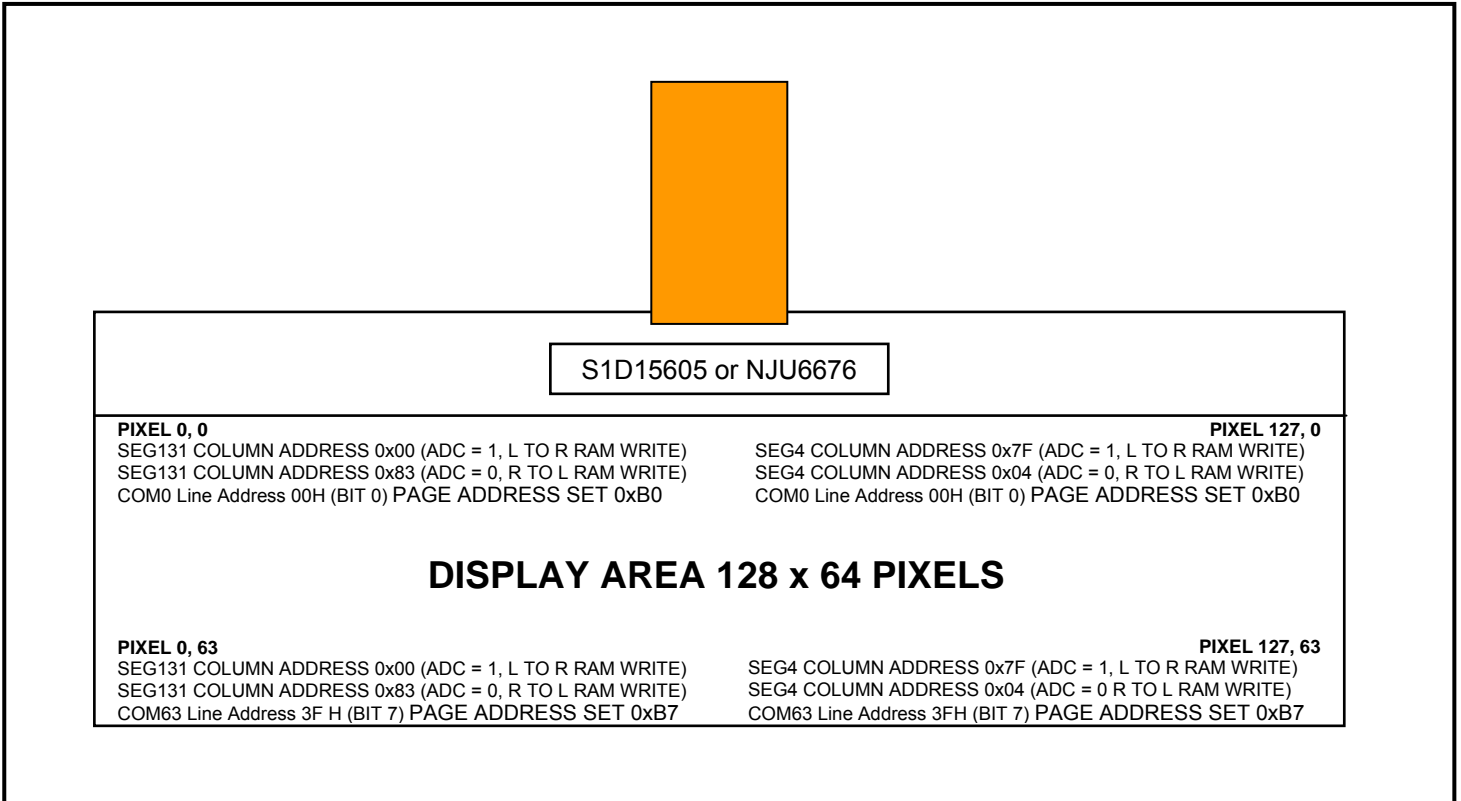
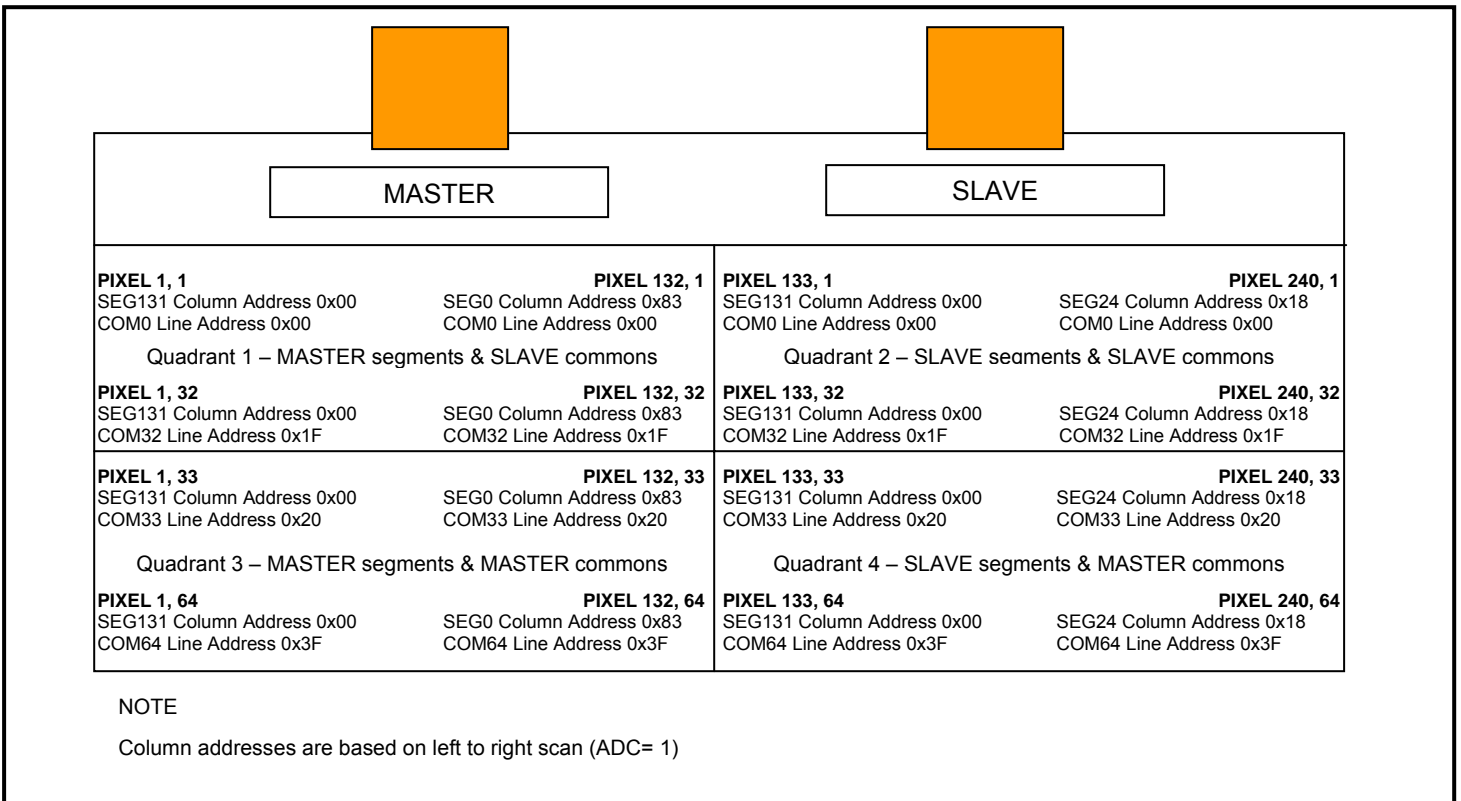


FIGURE 12 -- F-51405 & F-51851 PIXEL TO RAM MAPPING & ITO CONNECTIONS



6.4. SOFTWARE CONFIGURATION

Turn on $V_{DD} - V_{SS}$ while holding the RESET pin low. If supplying VLCD externally or supplying a voltage to the V_{OUT} pin, hold RESET low until all voltages stabilize. Note the power supply sequencing requirements for V_{DD} , V_{SS} and external voltages must be met.

Set RESET pin high. IC is initialized to default state.

Configure the IC with the following commands:

TABLE 2 – SOFTWARE CONFIGURATION COMMANDS

COMMAND NAME	VALUE	COMMENT
LCD BIAS SET	0xA2	Set LCD bias to 1/9 0xA2 1/9 bias 0xA3 1/7 bias
ADC SELECT	0xA1	Inverse scan (L to R) 0xA0 Normal Scan R to L 0xA1 Inverse Scan L to R
COMMON DIRECTION SELECT	0xC0	Scan commons top to bottom 0xC0 Normal scan top to bottom 0xC8 Inverse scan bottom to top
INITIAL DISPLAY LINE SET	0x40	Start COM scan at line address 00H 0x7F start COM scan at line 3FH Use this for scrolling
V_5 VOLTAGE REGULATOR RESISTOR RATIO SET	0x26	[COMMAND FOR S1D15605 ONLY] 0x26 for $(1 + (R_B/R_A)) = 6.0$ Use to set value of internal resistor ratio for electronic voltage regulator amplifier. NJU6676 uses external resistors.
EVR MODE SET	0x81	access the electronic volume register
EVR REGISTER SET	0x**	Set value of EVR to control contrast. Obtain values from graphs on pages 20 to 28. If a different V_{DD} or gain is selected, the user must calculate the desired EVR setting.
POWER CONTROL SET	0x2B	Recommended for F-51852 DC-to-DC Boost OFF, Voltage Regulator ON, Voltage Follower ON to provide software control of contrast. [F-51320 & F-51553] 0x2F to set DC-to-DC Boost ON, Voltage Regulator ON, Voltage Follower ON. [F-51405, F-51851, OR EXTERNAL POWER SUPPLY] 0x28 to set DC-to-DC Boost OFF, Voltage Regulator OFF, Voltage Follower OFF. These functions are performed by external power supply.
ENTIRE DISPLAY ON / OFF	0xA4	Normal display 0xA5 to turn on all pixels by overriding contents of RAM.

COMMAND NAME	VALUE	COMMENT
		RAM not affected. Use for testing.
LCD DRIVER ON / OFF	0xE7	[COMMAND FOR NJU6676 ONLY] Enable output drivers 0xE6 LCD drivers OFF 0xE7 LCD output drivers ON. THIS COMMAND NOT USED FOR S1D15605
LCD DISPLAY ON / OFF	0xAF	Display ON 0xAE display OFF. Power save mode 0xAF display ON
PAGE ADDRESS SET	0xB0	Select RAM page 0 to start writing at pixel 0 vertically.
COLUMN ADDRESS SET	0x10	Set upper 4 bits of column starting address to 00H.
COLUMN ADDRESS SET	0x00	Set lower 4 bits of column starting address to 00h. Display is now ready to begin RAM write at pixel 0, 0 in upper left corner and scan left to right.
WRITE DATA	0x**	data to be displayed. RAM column (horizontal) address will auto increment with each write. Reset column at end of horizontal row.

6.5. CONTROLLER / DRIVER CONFIGURATION & COMMISSIONING

- 6.5.1. Over time, commands to the controller may be corrupted by conducted or emitted noise (EMI) or electro-static discharges (ESD). The NJU6676 / S1D15605 does not use error detection and correction techniques to identify invalid commands. Using an invalid command may cause the controller to enter an undefined state. Periodically, a hardware RESET should be commanded to ensure a baseline configuration is attained. Follow up the RESET with a complete configuration and data image to ensure proper operation.
- 6.5.2. Execute the software RESET command more frequently than the hardware RESET to ensure proper configuration of the controller. Software RESET does not affect the data image.
- 6.5.3. During initial development, Optrex recommends using a parallel data interface which allows reading the S1D15605 status and RAM. The STATUS READ command returns the BUSY FLAG condition which is used to determine if the microprocessor is communicating with the controller and whether the controller able to accept data/commands. This feature is useful during development for confirming that EMI or ESD are not corrupting data. Once stability is demonstrated, the busy flag check may be removed.

Alternative methods for confirming correct communication are:

- Execute an ELECTRONIC VOLUME SET command and verify the voltage on V_5 changes as expected. An A/D converter is required.
 - Perform a data write and then execute a data read to confirm receipt. This is not possible with SPI interface.
- 6.5.4. The controller instructions require time to execute. While instructions are executing, commands and data should not be sent. The BUSY FLAG status is read by using the STATUS READ command. If the software design does not examine this bit, such as in SPI interface, the T_{CYC} requirements must be met to ensure adequate time for the NJU6676 /

S1D15605 to act upon commands. See pages 8-25 and 8-26 of reference (a) and page 31 of reference (b). T_{CYC} defines the fastest rate at which data can be sent to the controller.

Please note that the system cycle time varies with host type and logic voltage.

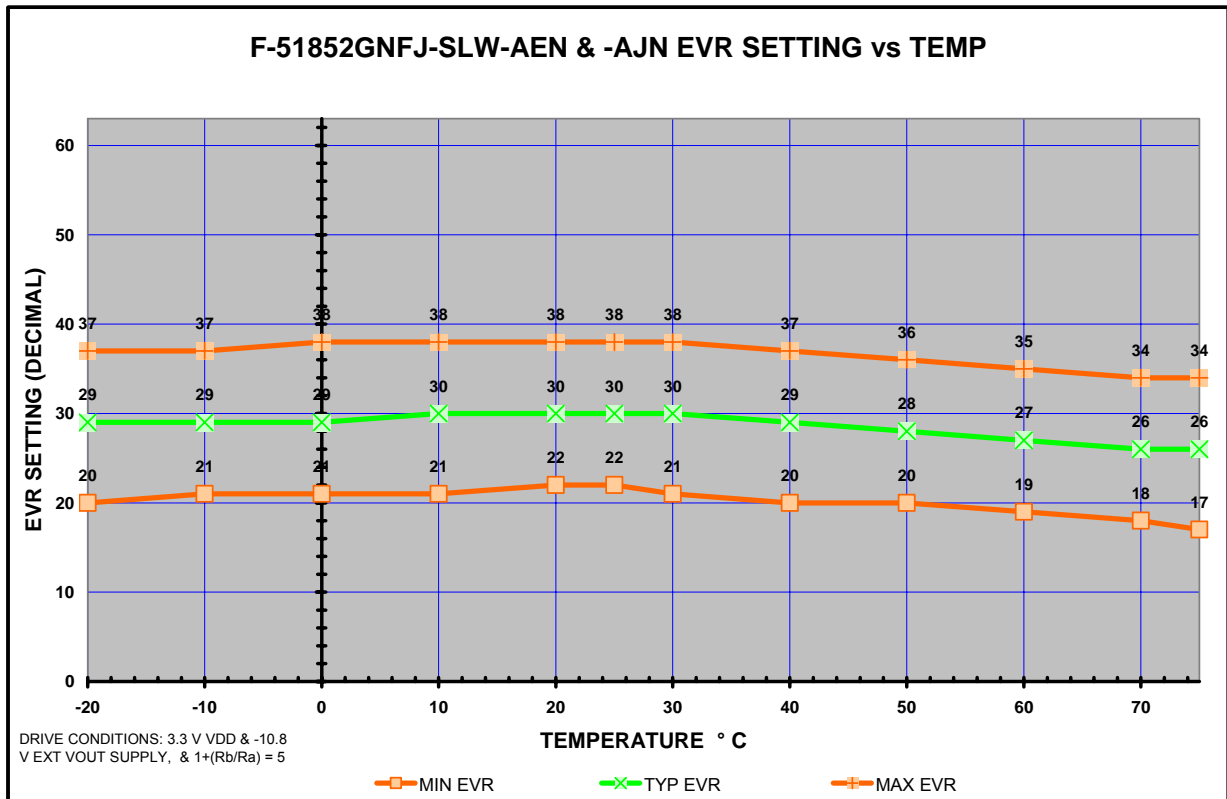
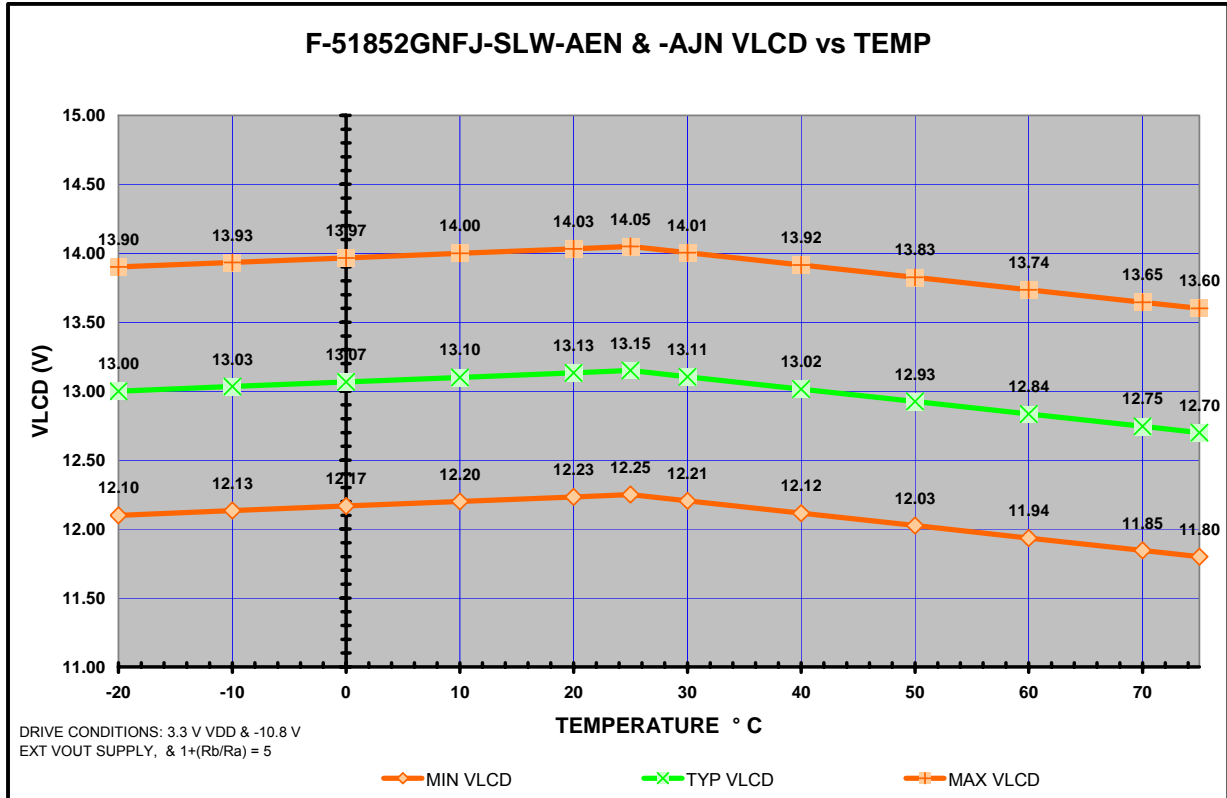
- 6.5.5. The fastest RAM image update rate, T_{CYC} , is significantly faster than the liquid crystal response speed. There are two liquid crystal response speeds: T_{RISE} and T_{FALL} , whose values are given in Section 3.2 of the LCD module specification. A typical total response time is 200 mS T_{RISE} and 240 mS T_{FALL} . Writing to the display with data that alternates state (1...0...1...0...) to the same RAM location will cause the pixel to not achieve the full ON or OFF light transmittance level. Contrast ratio will decrease and the image may appear fuzzy.

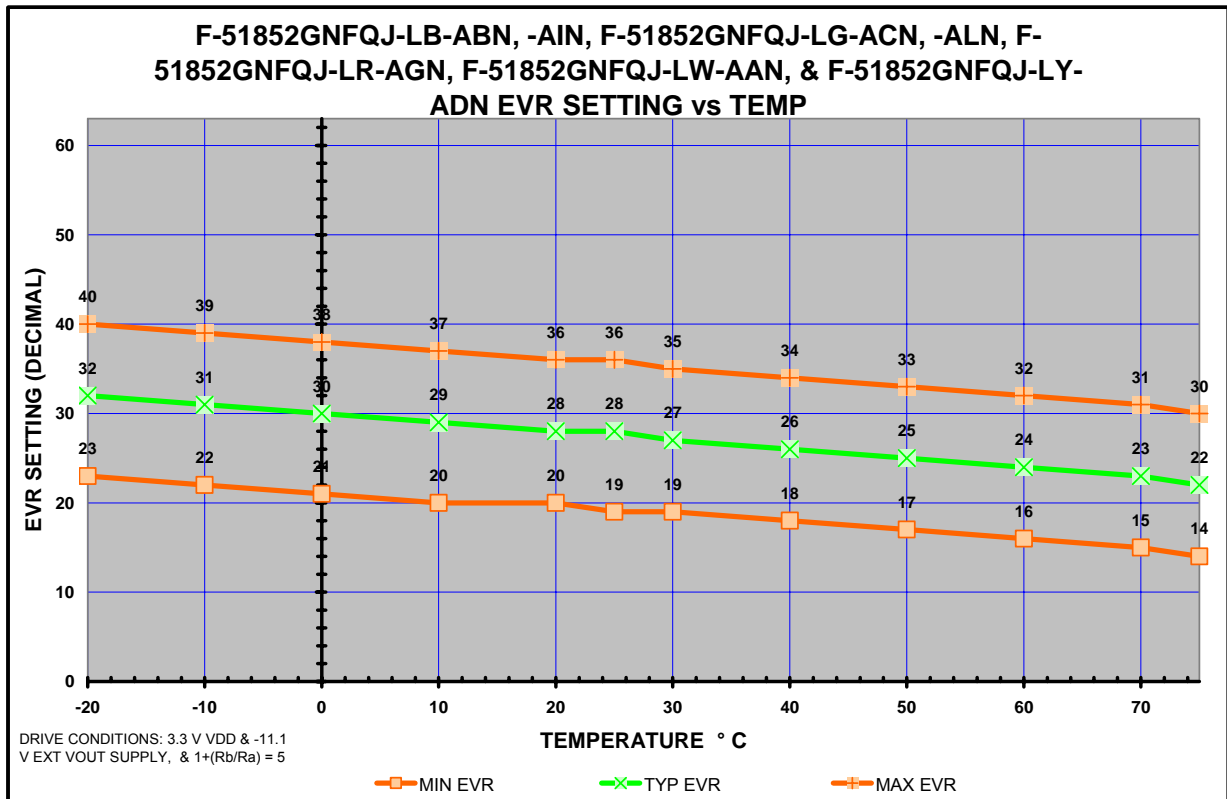
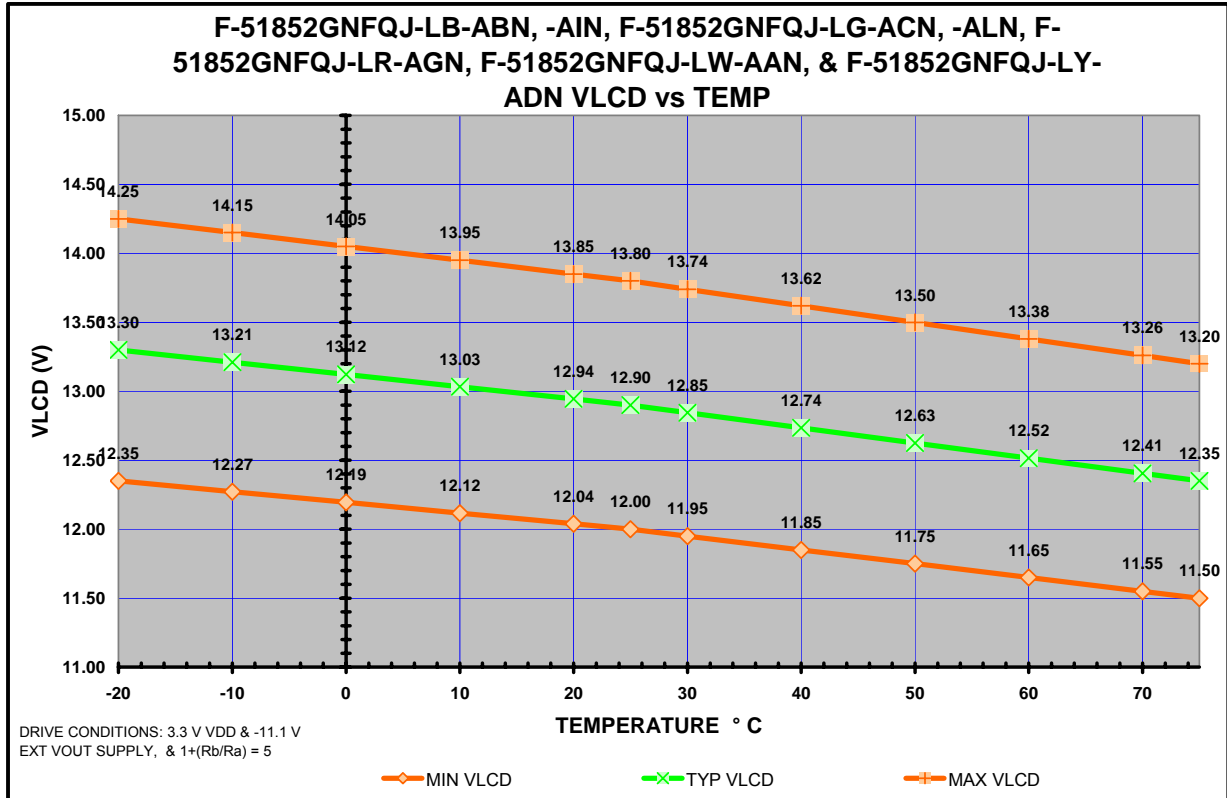
To achieve full contrast ratio performance, the image data should not be updated faster than the rate defined by $2 / (T_{RISE} + T_{FALL})$. For the data above, this rule of thumb suggests the image change rate is $2 / 0.440 \text{ S} = 4.54$ video frames per second.

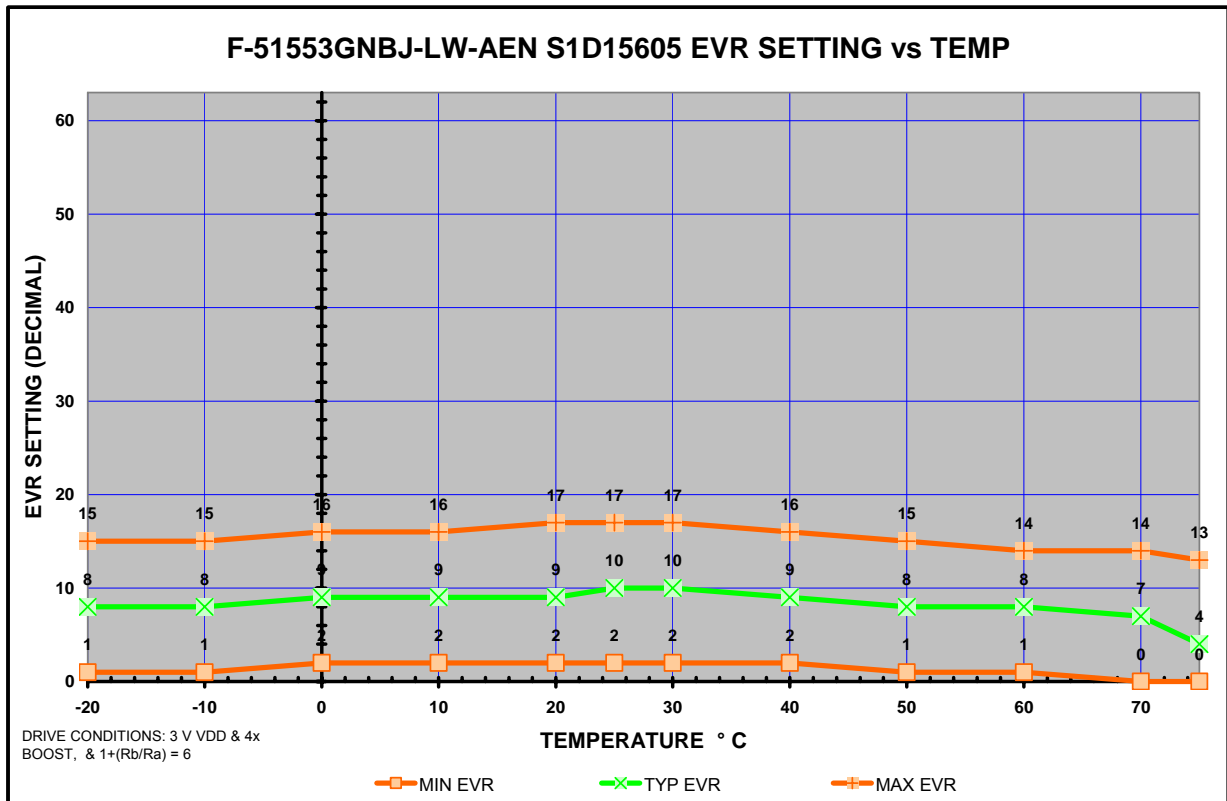
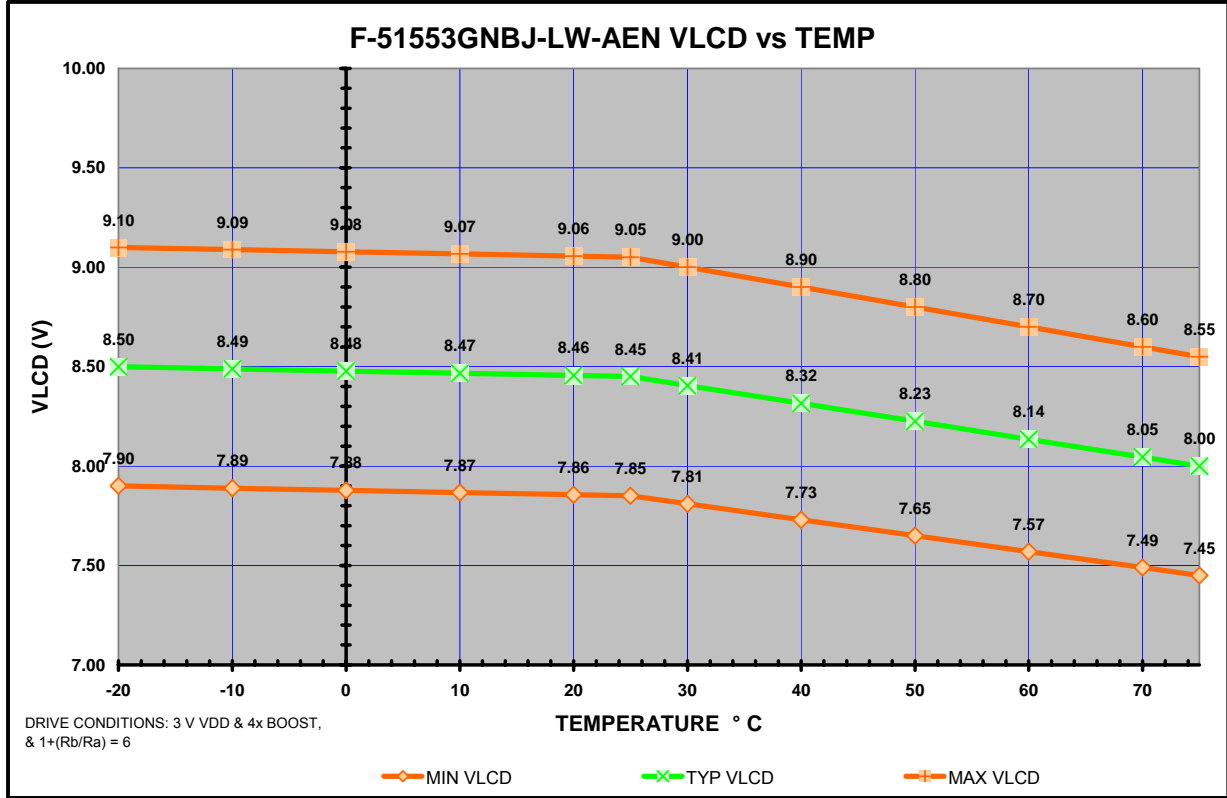
Faster image update is possible, but contrast performance will be sacrificed.

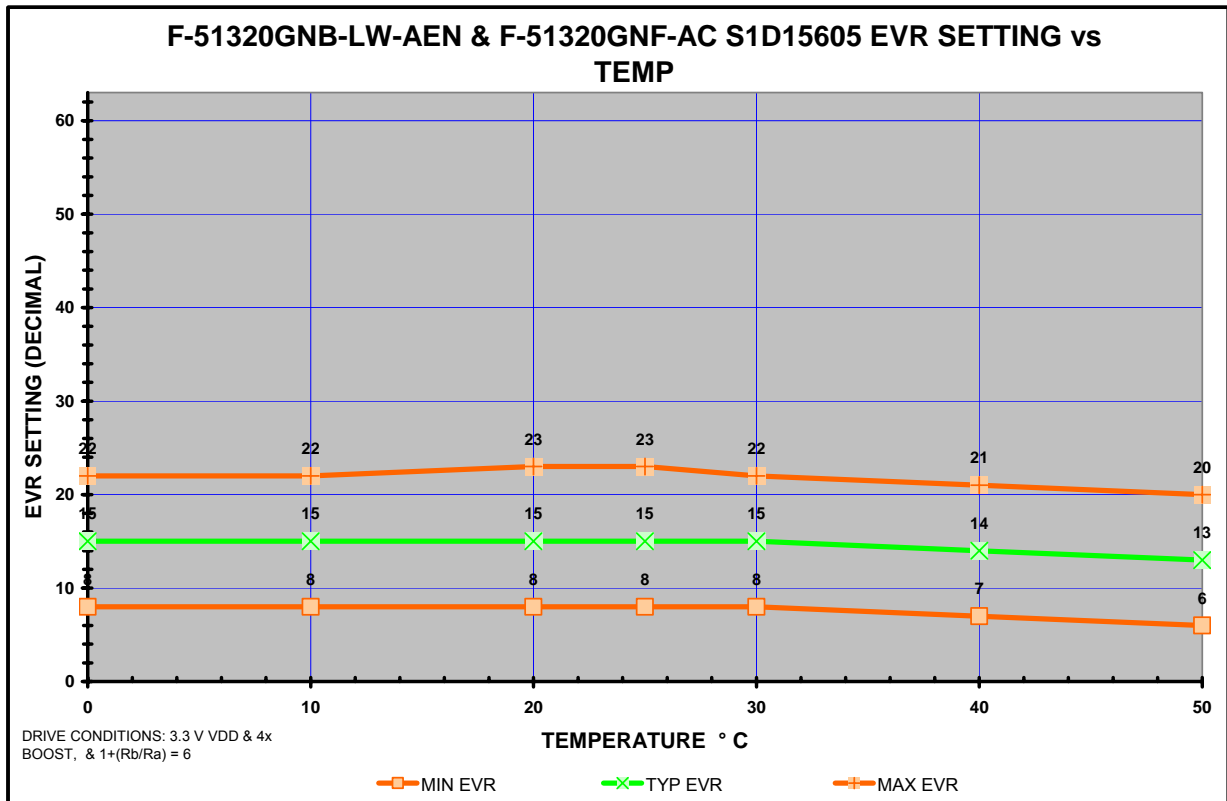
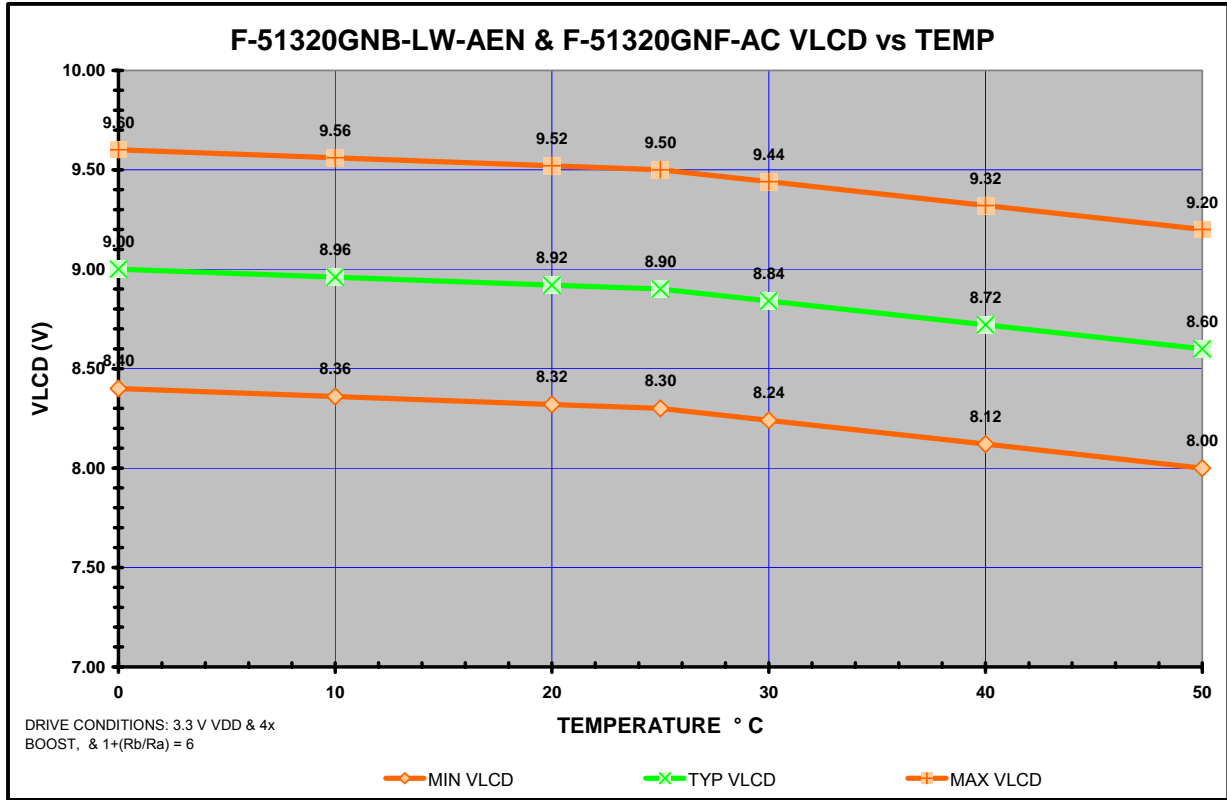
6.6. RECOMMENDED ELECTRONIC VOLUME REGISTER SETTINGS FOR CONTRAST CONTROL

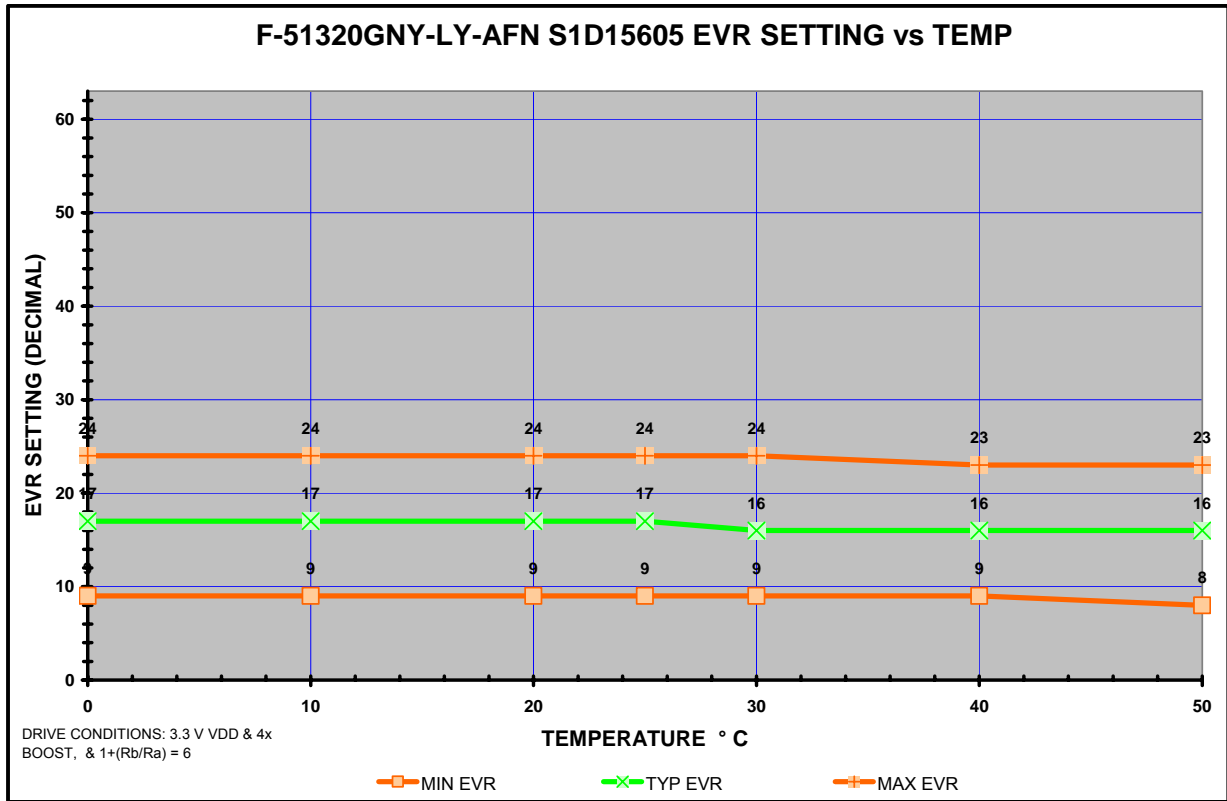
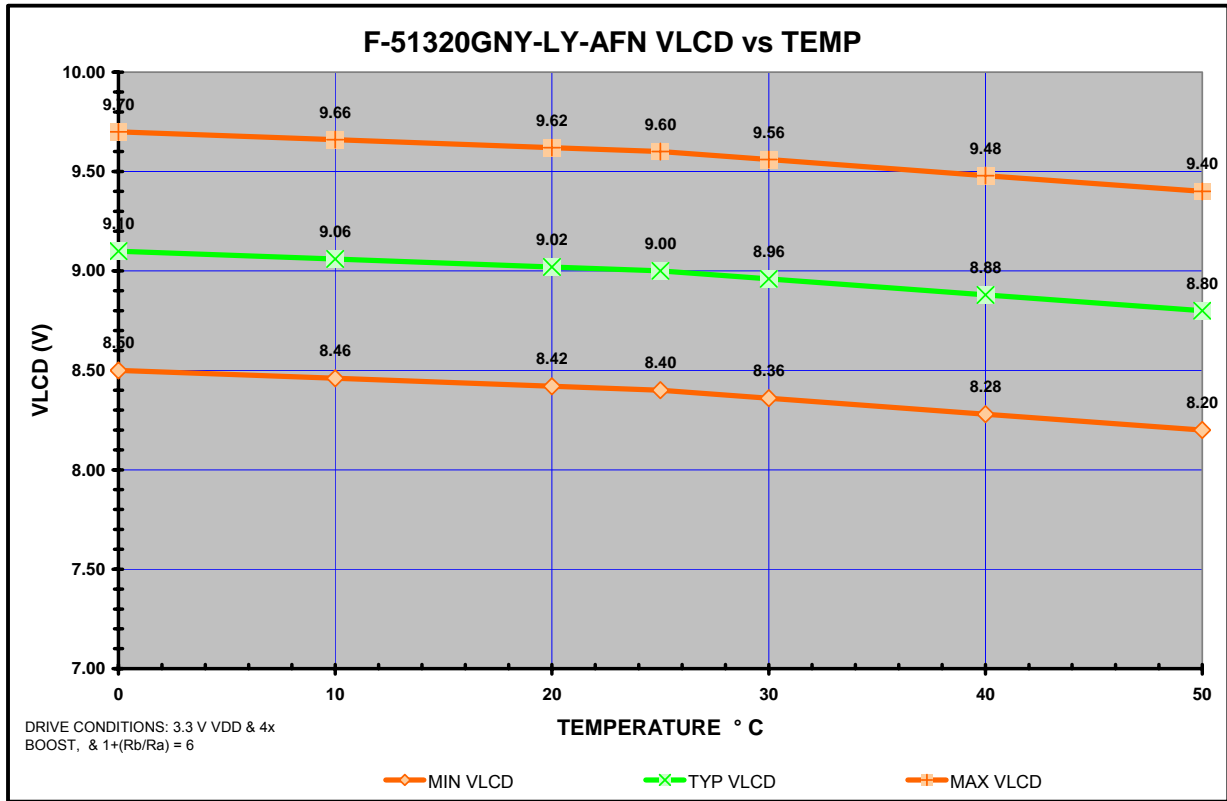
- 6.6.1. The following figures on pages 20 through 28 show the relationship between VLCD and temperature for proper contrast as well as ELECTRONIC VOLUME SET and temperature. Please note drive conditions in the lower left corner. These settings were calculated. If the $(1 + (R_A / R_B))$ amplification ratio is varied, the results will differ.
- 6.6.2. The EVR graphs are the production variation limits. Most displays will have an optimal setting much narrower than the range suggested by these graphs (see FIGURE 2 for an explanation). A robust system design and production process accomodates this variation by:
- Retaining the optimal 25° C EVR setting in memory. This value is set at the factory. This reduces optical variation and ensures all displays have similar appearance.
 - Limits the low EVR setting to prevent adjusting the pixel voltage too low (all pixels OFF condition – no image). This setting prevents customers from adjusting to a point they cannot see an image.
 - Limits the high EVR setting to prevent adjusting the pixel voltage too high (all pixels ON condition – no image). This setting prevents customers from adjusting to a point they cannot see an image.



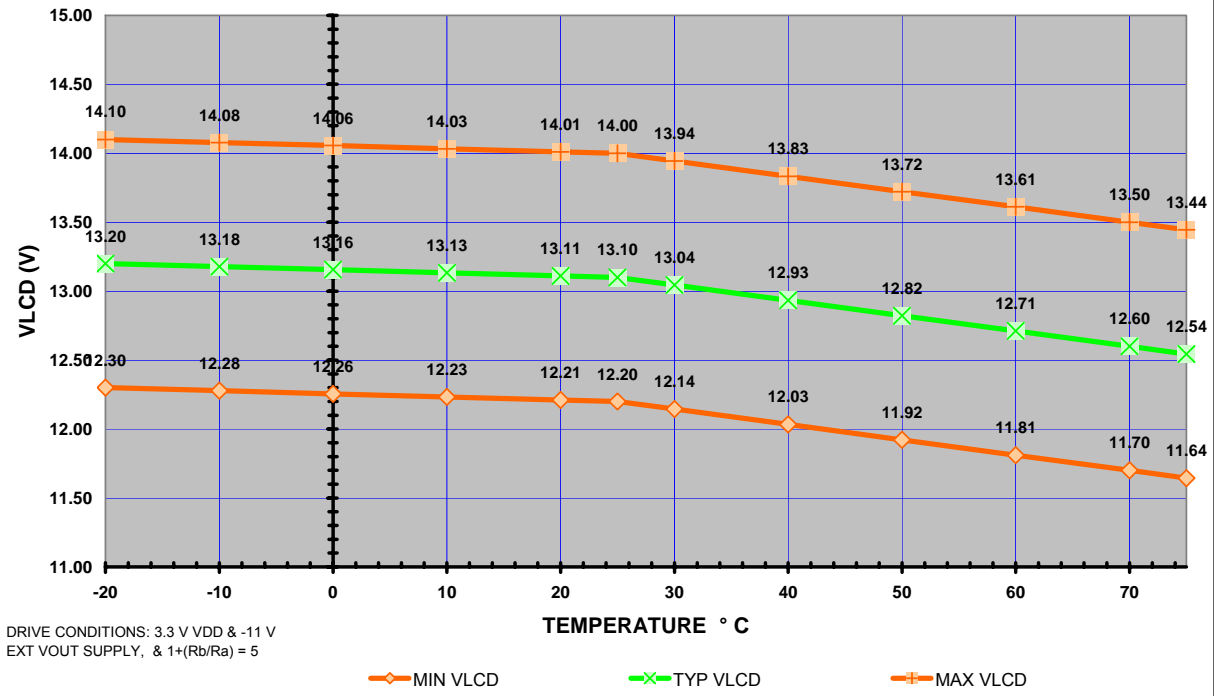




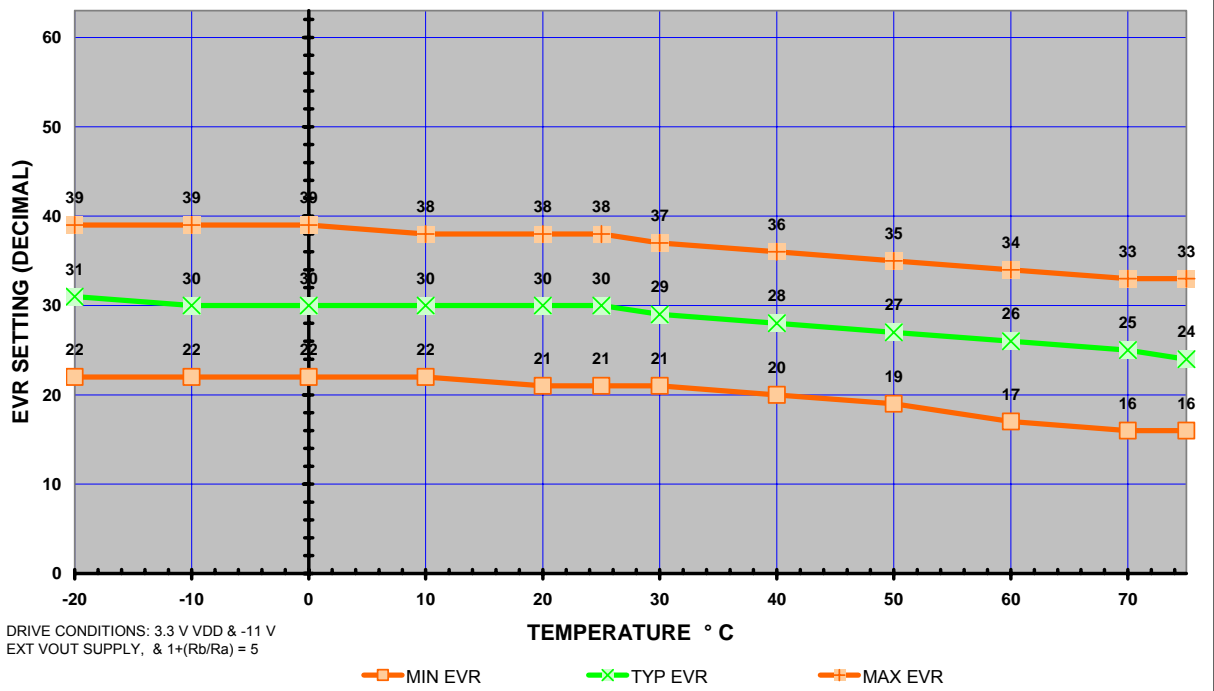


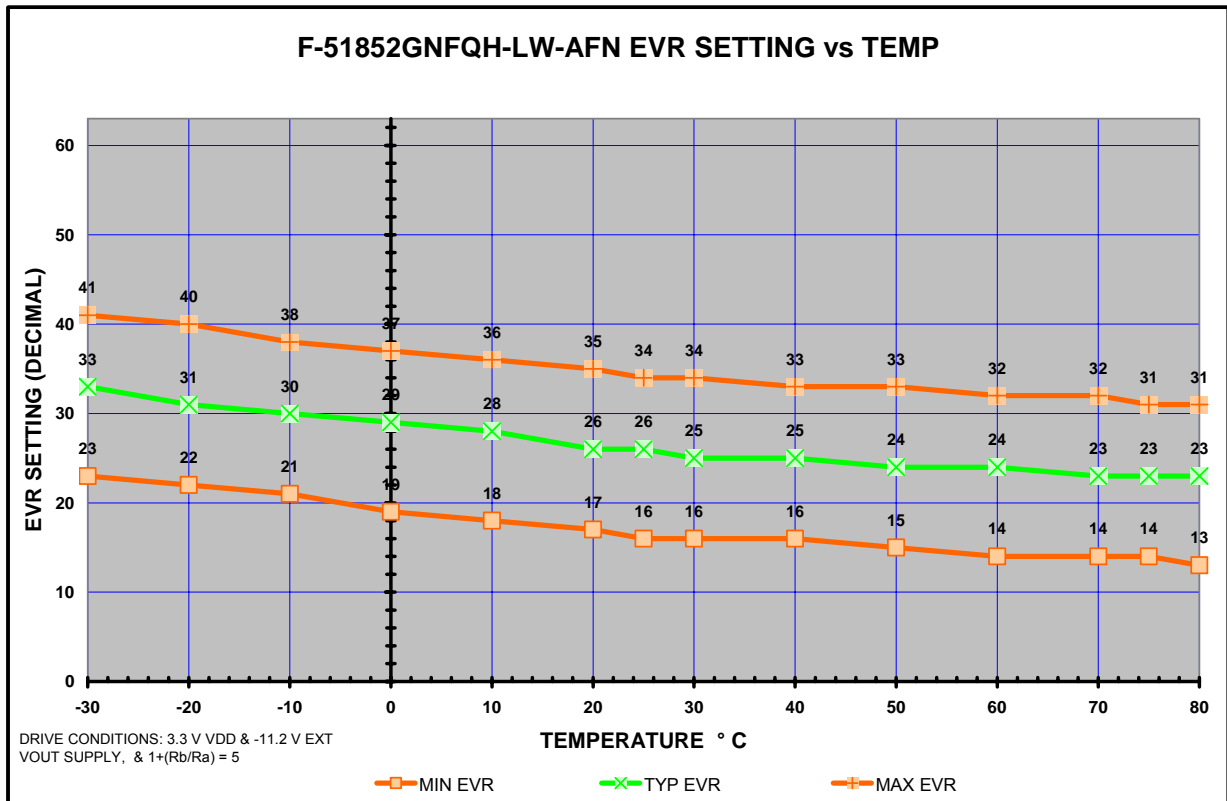
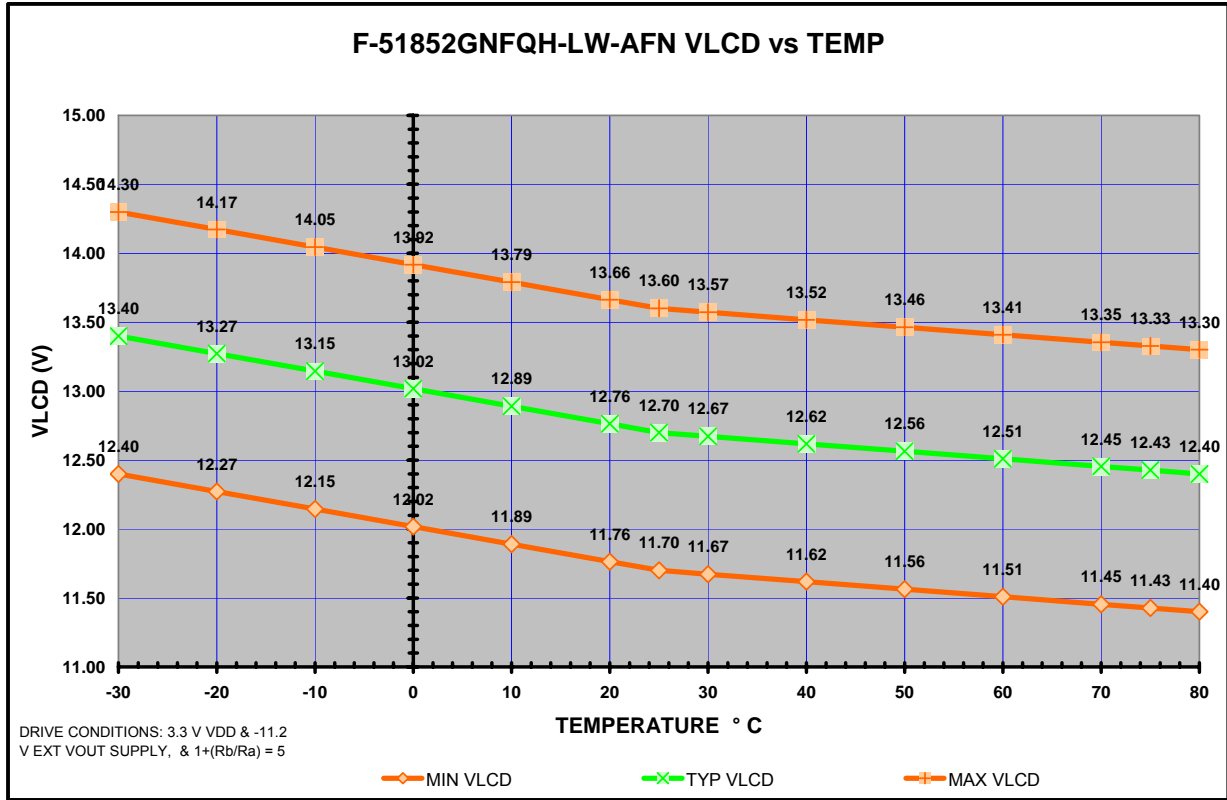


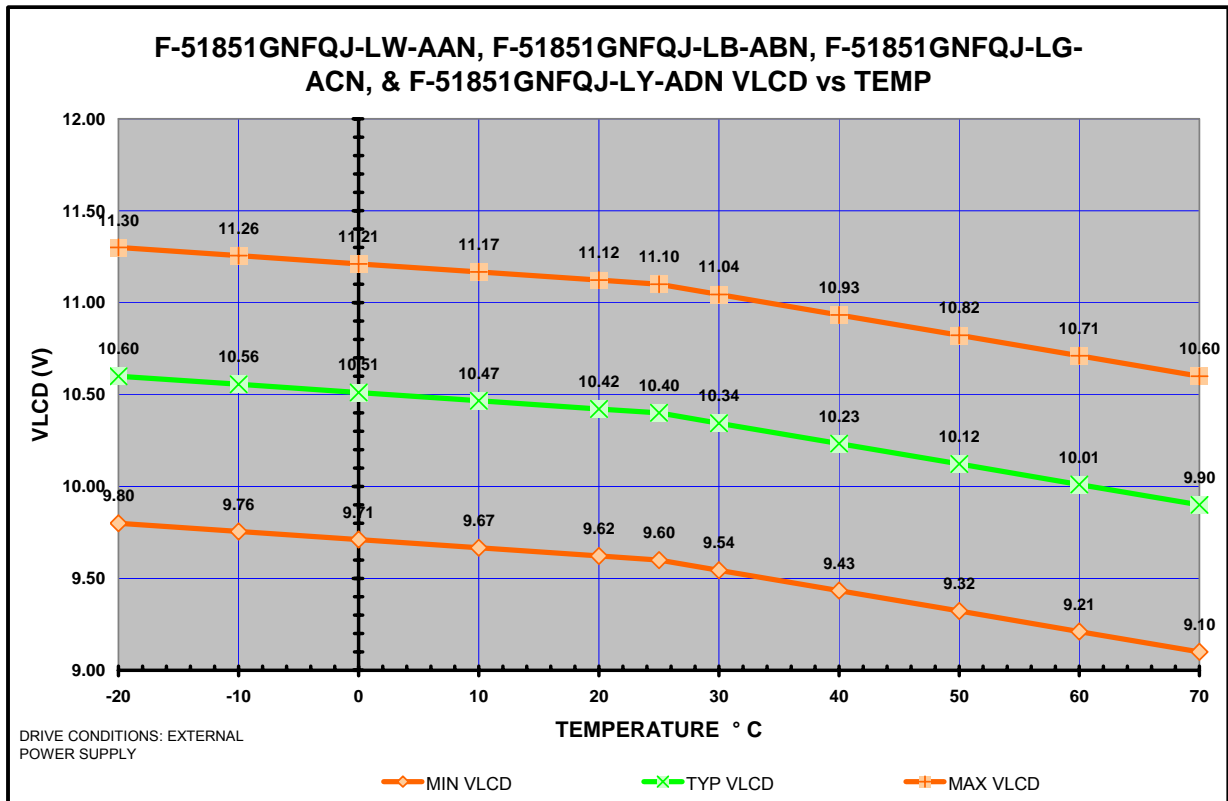
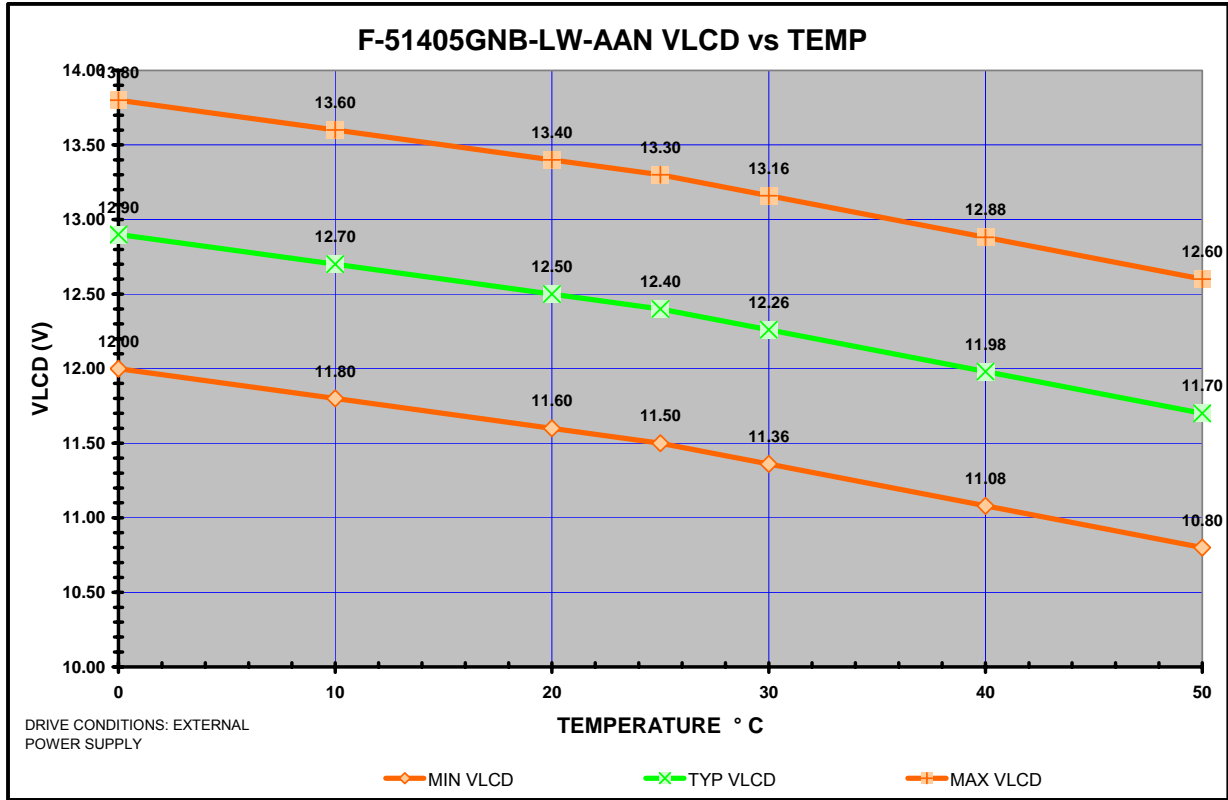
F-51852GNBJ-LW-AKN & F-51852GNBJ-LW-AMN VLCD vs TEMP



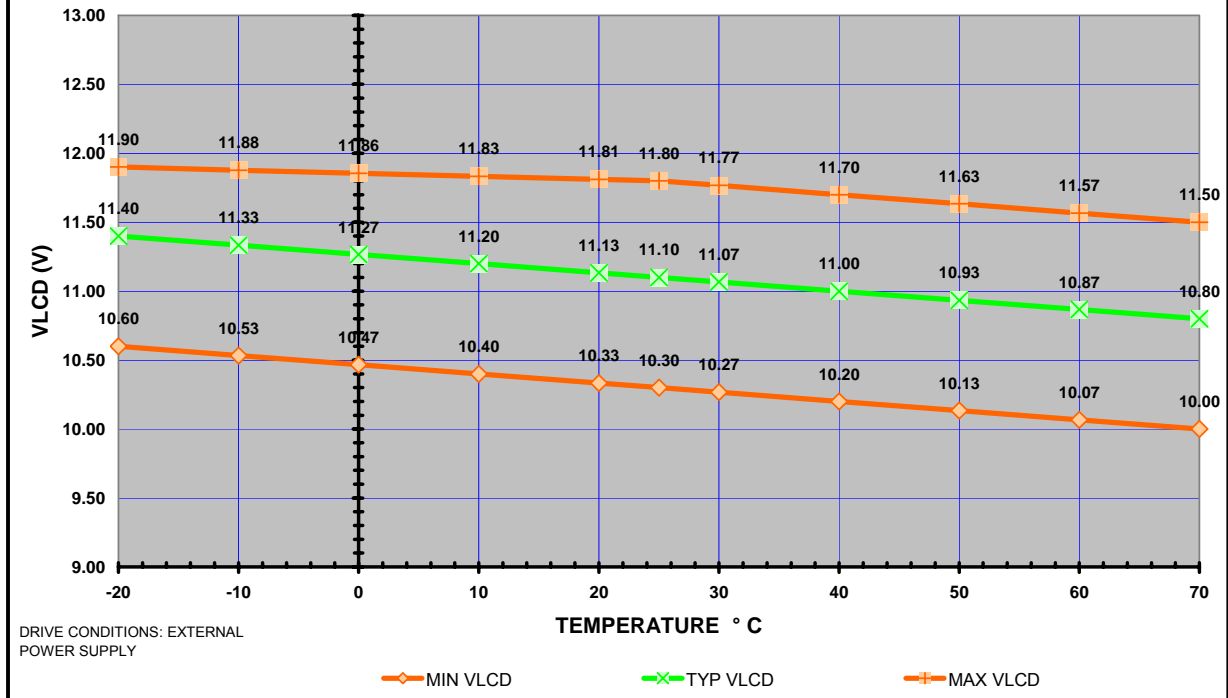
F-51852GNBJ-LW-AKN & F-51852GNBJ-LW-AMN EVR SETTING vs TEMP







F-51851GNFJ-SLW-AEN VLCD vs TEMP



7.0 HANDLING RECOMMENDATIONS

7.1. FPC HANDLING PRECAUTIONS

- DO NOT pick the display up by the FPC tail. This action can break the electrical connection to the glass or peel the FPC away.
- DO NOT PULL the FPC. This action can break the electrical connection to the glass or peel the FPC away.
- DO NOT BEND THE FPC UPWARD from the glass surface. This will break the electrical connection to the glass.
- DO NOT BEND THE FPC TIGHT and form creases. This will fracture the copper traces and cause an open circuit.
- ALWAYS bend the FPC so the bend applies a compressive force to the FPC to GLASS bond area.

7.2. LCD PROTECTIVE LINER

- The display is manufactured with an optical-grade, clear protective liner attached to the front polarizer. The liner is optical grade to allow inspection through the liner while it is still attached.
- Leave the liner installed until the last possible moment in production to protect the polarizer from impact scratches, fingerprints, and airborne debris.
- Remove the protective liner by placing a small piece of adhesive tape at a corner and press it in place. SLOWLY use the tape to pull the protective liner up and roll off the glass. The protective liner should bend 180° back upon itself as it is slowly pulled. A slow pulling speed reduces electrostatic voltage activating the pixels.

8.0 PROTOTYPING RECOMMENDATIONS

8.1. The display interface is via ZIF connector making it difficult to construct hand-built prototypes. A source for ZIF to wire breakouts for prototyping is [Quadrangle Products](#).

8.2. Adapter part numbers for F-51320, F-51553, and F-51852 are:

[Quadrangle RT-700G-30-DIS](#) – 30 Conductor, 0.5 mm pitch, FPC to discrete wire adapter.

[Quadrangle QD7018C](#) – 30 Conductor, 0.5 mm pitch, female to female ZIF adapter. This product plugs into the display ZIF and RT-700G-30-DIS converting 30 conductor, 0.5 mm pitch FPC to discrete wire.

8.3. Quadrangle does not make a 36-pin adapter. You must use a 45 pin adapter and position the flex against one side leaving nine pins not connected. Adapter part numbers for F-51405 and F-51851 are:

[Quadrangle RT-700G-45-DIS](#) – 45 Conductor, 0.5 mm pitch, FPC to discrete wire adapter.

[Quadrangle QD7018-45C](#) – 45 Conductor, 0.5 mm pitch, female to female ZIF adapter. This product plugs into the display ZIF and RT-700G-30-DIS converting 45 conductor, 0.5 mm pitch FPC to discrete wire.

9.0 SPECIFICATION ERRATA

The following sections provide corrections to the specifications.

END_OF_FILE