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Type No **F-51405-Series 5.2-inch, 240x64 Monochrome**		Approved By Customer

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REVISION HISTORY

REV	DATE	PAGE	COMMENT

1.0 REFERENCES

1.1. Seiko Epson Document MF424-21 S1D15000 Series Technical Manual
http://www.epsondevice.com/domcfgen.nsf?OpenDatabase

1.2. Optrex Drawing UE-311744-00 F-51405GNB-LW-AJ dated 21 February 2003.
http://www.optrex.com/SiteImages/PartList/DRAWING/drawing of F-51405AJ.pdf

1.3. Document 2003-0122 F-51405GNB-LW-AJ LCD Module Technical Specification Rev. First Edition dated 7/23/2004.
http://www.optrex.com/SiteImages/PartList/SPEC/F-51405GNB-LW-AJ-final.PDF

1.4. Optrex Drawing UE-310700C F-51405GNY-LY-AB dated 15 February 2002.
http://www.optrex.com/SiteImages/PartList/DRAWING/F51405abd.pdf

1.5. Document 2002-0061 F-51405GNY-LY-AB LCD Module Technical Specification Rev. First Edition dated 20 February 2002.
http://www.optrex.com/SiteImages/PartList/SPEC/F-51405GNB-LW-AJ-final.PDF

2.0 DESCRIPTION

2.1. This application note provides guidance for interfacing, programming, and using the F-51405 family of displays. This document, along with references 1.1 through 1.5, provides the application information needed design the display into electronic products. This document IS NOT INTENDED to be the sole source of guidance for using the display.

2.2. The F-51405 displays include the following components:

Liquid crystal display cell

S1D15605 LCD Controller / Driver (2) configured as MASTER and SLAVE.

Display RAM

Backlight / Carrier

2.3. The MASTER and SLAVE controller-drivers each drive one-half of the LCD screen. The microprocessor accesses each controller independently to configure and display data. The MASTER provides synchronization signals to the SLAVE for proper operation. The display requires an external power supply for contrast control. Reference 1.1 describes how to use this device. Optrex highly recommends users download reference 1.1 and read the section on the S1D15605 before designing hardware and software.

3.0 ELECTRICAL

3.1. Interface Connection & Voltages

3.1.1. The interface to the display are through two 36-conductor flexible printed circuits (FPC). Sources for compatible connectors are:

AVX Elco 08-6210-036-340-800 – 36 pin, zero insertion force (ZIF), right angle, bottom contact, surface mount, 0.5 mm pitch FPC, 0.30 mm thick.

Molex 54132-3690 – 36 pin, zero insertion force (ZIF), right angle, bottom contact, surface mount, 0.5 mm pitch FPC, 0.30 mm thick

3.1.2. The S1D1505 controller/drivers may be configured for 8-bit parallel or 8-bit serial (SPI) communication. Selection of this option is controlled by the P/S pin (34). Use of serial communication prevents reading the display status and RAM. It is often advantageous to use the parallel interface during development in order to poll controller status. Once the design is known to not have ESD or EMI/EMC issues causing communication problems, then switch to the serial interface.

3.1.3. Pin (34) P/S – pull the pin high or low; do not float. Pull the pin high for parallel data input or LOW for serial data communication. Floating the pin is known to cause timing issues. The pin must be set the same for MASTER (CN1) and SLAVE (CN2).

3.1.4. If set for serial (SPI) interface, use the following connections in lieu of those shown in Figure 1. See reference 1.1 page 8-25.

Pins 11 to 16 (D0 to D5) – no connect

Pin 17 D6 – Serial clock (SCL)

Pin 18 D7 – Serial data (SI)

3.1.5. Pin (35) IRS – The IRS pin controls the usage of internal resistor values used for the DC to DC boost converter. This converter is not used since an external power supply will be used to create the LCD drive voltages. Pin 35 (IRS) should be set low for the MASTER. The IRS pin should not be connected for the SLAVE. The SLAVE pin is pulled to V_{DD} on the glass. Setting the SLAVE IRS low will cause the display contrast to vary by quadrant.

3.1.6. Pins (2) FR, (3) CL, (4) DOF – The MASTER outputs clock and frame signals to the SLAVE for synchronization purposes. These pins should be connected together from the MASTER to SLAVE using the shortest possible path length to minimize capacitance that can distort the timing waveforms. The DOF pin allows the MASTER to control the SLAVE output driver pins ON and OFF.

3.1.7. Do not connect the boosting capacitor pins (22 to 26).

3.1.8. The S1D15605 is selected when CS1 is low and CS2 is high. Please note the MASTER and SLAVE must not be selected simultaneously.

3.2. Power Supply

3.2.1. The Optrex specification lists the S1D15605 as 5 V logic operation, but the IC operates at 1.8 V to 5 V logic levels. The user must set V_5 appropriately to generate the V_{DD}-V_5 voltage difference to run the liquid crystals.

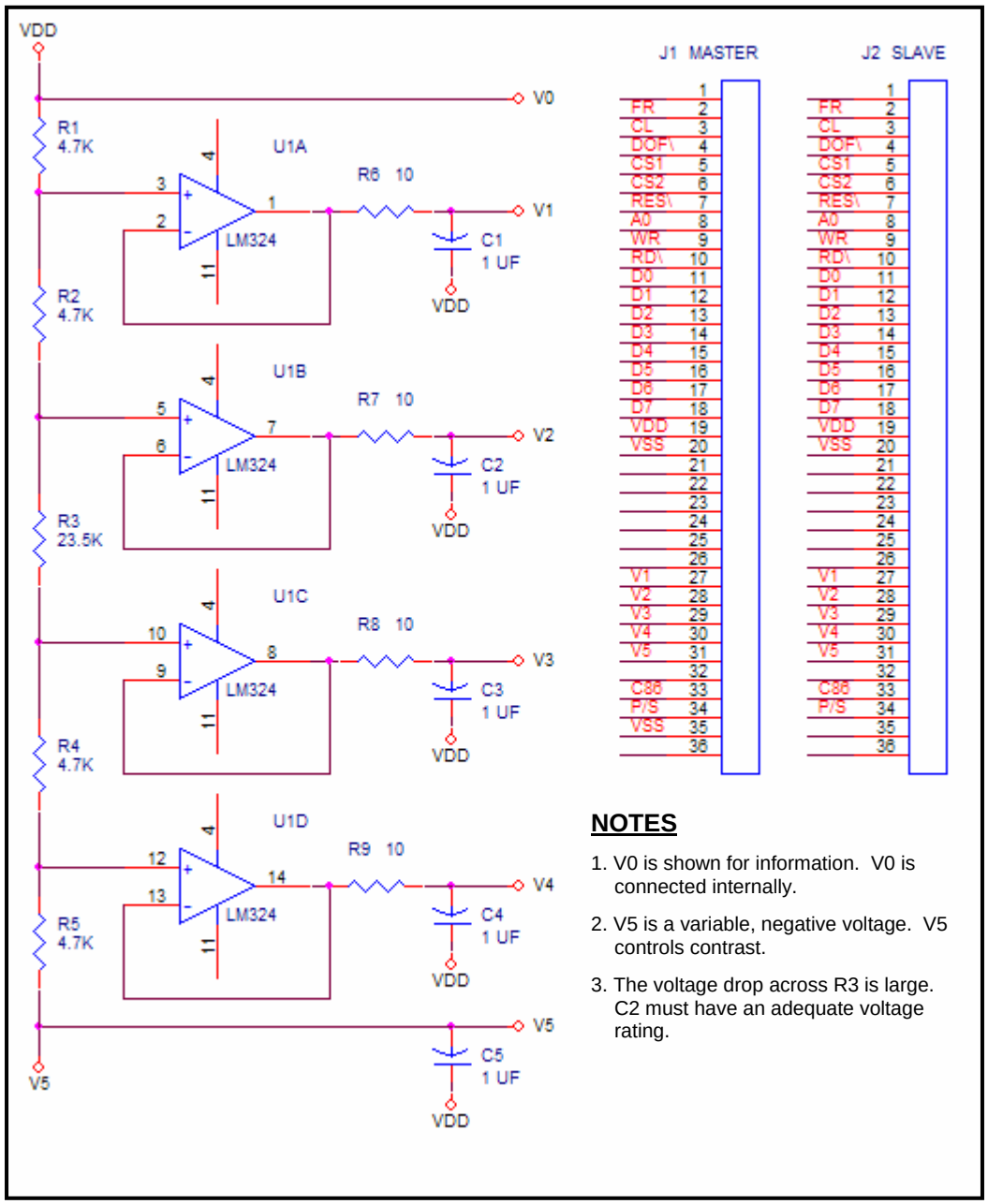
3.2.2. The S1D15605 is negatively biased; V_{DD} is used as the reference voltage. The difference between V_{DD} and the LCD drive voltage (V_5) must meet the requirements of Section 3.1 of the LCD specifications.

3.2.3. The S1D15605 has an internal boost circuit to generate the LCD drive voltages. In SLAVE mode, the power supply section is disabled preventing DC boosting. The SLAVE IC configuration is fixed and cannot be changed. The MASTER DC/DC converter has insufficient power to drive the F-51405 panel reliably. Optrex recommends using an external power supply to generate V_5. V_5 is negative voltage such that V_{DD}-V_5 equals the V_{LCD} drive voltage requirement.

3.2.4. Section 3.1 of the display specification lists the variation of V_{LCD} over temperature for control of contrast. The V_5 voltage must be adjustable to provide proper contrast over the operating temperature range.

3.2.5. Figure 1 provides a reference hookup of power suppy and I/O.

Figure 1 -- F-51405 Power Supply & I/O Connections



3.3. Signal Timing

3.3.1. S1D15605 timing varies with the operating voltage. Please consult reference 1.1 if you intend to use V_{DD} other than 5 V.

3.3.2. RESET timing is important; please follow the specification guidance.

3.3.3. The S1D15605 instructions require some time to execute. While instructions are executing, commands and data should not be sent. The status of the controller can be read with a parallel interface by using the STATUS READ command to return the

BUSY FLAG value. If the software design does not examine this bit, the T_{cyc} requirements must be met to ensure adequate time for the S1D15605 to act upon commands. See pages 8-25 and 8-26 of reference 1.1.

3.4. Backlight

3.4.1. The backlight uses a JST PHR-2 connector. This is a removable, 2 mm pitch, crimp pin connector using the PHR-2 housing. The mating connector is a 2-pin header.

JST S 2B-PH-SM3-TB – 2-pin, surface mount, side entry, shrouded header, 2 mm pitch.

3.4.2. The F-51405GNB-LW-AJ has current limiting resistors to protect the LEDs. The user may connect the LED drive voltage directly to the anode and cathode.

The F-51405GNY-LY-AB does not use current limiting resistors. The user must provide a current limiting resistor to protect the LEDs. The resistor must meet the criteria of Equation 1 and have adequate power rating.

Equation 1 – Current Limiting Resistor Calculation

$$\frac{V_{SUPPLY} - V_f}{R} \leq I_f$$

3.4.3. The values of V_f and I_f are found in Section 2.4.2 of references 1.3 and 1.5. PWM techniques may be used to control luminance. The high temperature current deratings must be followed.

3.5. Power Supply Sequencing & Signal Transients

3.5.1. The external power supply should be sequenced so that the voltage comes up after V_{DD} at startup and shuts down before V_{DD} at power down. This sequencing should be maintained for inadvertent power down as well. The sequencing relationship depends upon the V_1 to V_5 capacitance and V_{DD}. See reference 1.1 pages 8-58 through 8-63 and Figure 29.

3.6. PCB Layout Requirements

3.6.1. The CLK, DOF, and FR signal traces between the MASTER and SLAVE connections should be kept as short as possible to minimize signal degradation.

4.0 SOFTWARE

4.1. RAM Mapping

4.1.1. Reference 1.1 pages 8-27 and 8-28 discuss the LCD controller RAM operation. The mapping of pixels to RAM and S1D15605 outputs is shown in Figure 2. The MASTER RAM stores the left half of the image and the SLAVE RAM stores the right half.

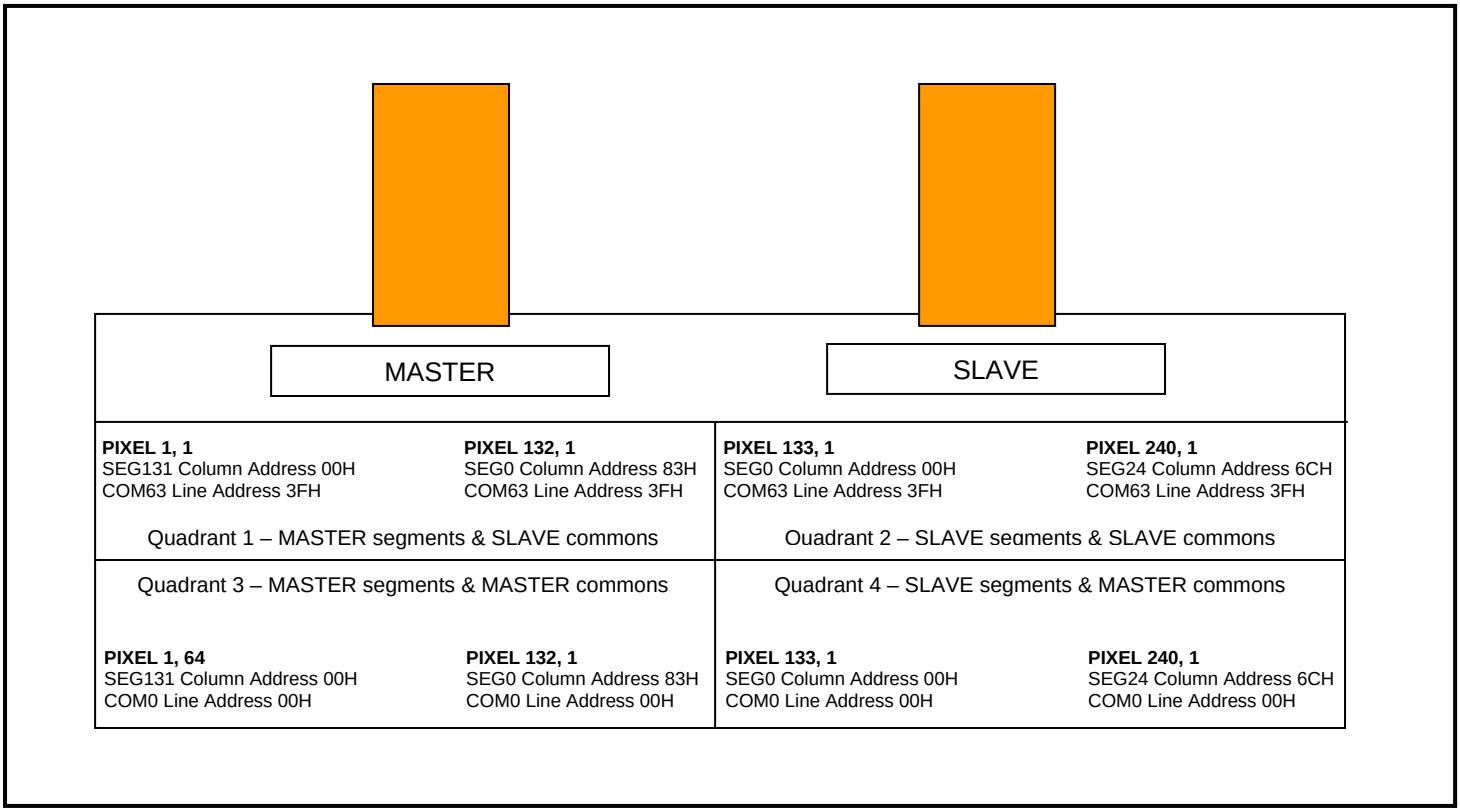
4.1.2. Given the pixel mapping of Figure 2, a left to right and up to down image scan requires setting the ADC SELECT register value to 0xA1 to reverse the horizontal scan and the COMMON OUTPUT MODE SELECT register value to 0xC8 to reverse the vertical scan.

4.1.3. Unused RAM locations in the S1D15605 may be used for scratchpad memory. Unused RAM locations are:

SLAVE PAGES 1 to 7 Column Addresses 6DH to 83H

MASTER and SLAVE PAGE 8

Figure 2 -- Pixel to RAM Mapping & ITO Connections



4.2. Controller / Driver Configuration

4.2.1. Over time, commands to the S1D15605 may be corrupted by conducted or emitted noise (EMI) or electro-static discharges (ESD). The S1D15605 does not use error detection and correction techniques to identify invalid commands. Using an invalid command may cause the controller to enter an undefined state. Periodically, a hardware RESET should be commanded to ensure a baseline configuration is attained. Follow up the RESET with a complete configuration and data image to ensure proper operation.

4.2.2. Execute the software RESET command more frequently than the hardware RESET to ensure proper configuration of the controller. Software RESET does not affect the data image.

4.2.3. During initial development, Optrex recommends using a parallel data interface which allows reading the S1D15605 status and RAM. The STATUS READ command returns the BUSY FLAG condition which is used to determine if the microprocessor is communicating with the controlller and whether the controller able to accept data/commands. This feature is useful during development for confirming that EMI or ESD are not corrupting data. Once stability is demonstrated, the busy flag check may be removed.

4.2.4. The S1D15605 instructions require some time to execute. While instructions are executing, commands and data should not be sent. The BUSY FLAG status is read by using the STATUS READ command. If the software design does not examine this bit, the T_{cyc} requirements must be met to ensure adequate time for the S1D15605 to act upon commands. See pages 8-25 and 8-26 of reference 1.1. T_{cyc} defines the fastest rate at which data can be sent to the controller.

4.2.5. References 1.31.3 and 1.5 Section 2.3.3 provides a suggested initialization sequence. Please follow the sequence titled **"When built-in power supply is not being used after turning on power."** The numbers in parentheses identify the number of the command in reference 1.1 section 7 "Commands." Please note the following:

4.2.5.1. The internal power supply section is not being used; the bias ratio is set by the external power supply resistor divider network to (1/9) Software conifguration of the (11) LCD BIAS SET register to 0xA2 (1/9) is not required.

4.2.5.2. The internal power supply section is not being used. Configure the (16) POWER CONTROLLER SET register to 0x28 to turn the DC to DC boost circuit OFF, turn the voltage regulator OFF, and turn off the voltage follower OFF.

4.2.5.3. The (17) V_5 VOLTAGE REGULATOR INTERNAL RESISTOR RATIO SET is not used.

4.2.5.4. The (18) ELECTRONIC VOLUME SET command is not effective since the power supply is not used. Set the ELECTRONIC VOLUME MODE SET register to 0x81 followed by the ELECTRONIC VOLUME REGISTER SET to 0x20 to turn the electronic volume control OFF.

5.0 SPECIFICATION ERRATA

5.1. The following sections provide corrections to references 1.3 and 1.5.

5.2. Section 2.3.3 Note 2 replace V_{SS} with V_{DD}.

5.3. Section 4.1
Pins 27 through 31 – Use the following description

NO	SYMBOL	FUNCTION
27	V_1	Power Supply for V_{LCD} drive $V_1 = 1/9(V_{DD}-V_5)$
28	V_2	Power Supply for V_{LCD} drive $V_2 = 2/9(V_{DD}-V_5)$
29	V_3	Power Supply for V_{LCD} drive $V_3 = 7/9(V_{DD}-V_5)$
30	V_4	Power Supply for V_{LCD} drive $V_4 = 8/9(V_{DD}-V_5)$
31	V_5	Power Supply for V_{LCD} drive $V_5 = 9/9(V_{DD}-V_5)$

Note: All voltages are referenced to V_{DD} not V_{SS}.

5.4. Section 4.1
Pin 32 – Replace V_{CC} with V_{DD}
Pin 35 – replace function with the following:

This terminal selects the resistors for the V_5 voltage level adjustment.
MASTER (CN1)
IRS = "H" : Use the internal resistors
IRS = "L" : Do not use the internal resistors. The V_5 voltage level is regulated by an external resistor divider attached to the power supply terminals.

SLAVE (CN2)
IRS = NC (IRS is pulled to V_{DD} on the glass)

5.5. Section 4.2 provides a power supply connection diagram. The picture does not show the SLAVE which should be connected similarly. The IRS pin is connected to GND for the MASTER; the SLAVE IRS pin should not be connected. The diagram shows the M/S pin which is set by the factory for the MASTER and SLAVE; this pin is not configurable by the user.